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PERFORMANCE ANALYSIS OF POWER GATING DESIGNS IN LOW POWER VLSI CIRCUITS

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ABSTRACT
With the rise of mobile devices, power consumption has become a pivotal design parameter in digital circuits. The primary contributor to power dissipation during idle mode is leakage currents, which have seen a significant increase due to threshold voltage scaling and the scaling of oxide thickness. As mobile devices predominantly operate in standby mode, minimizing leakage power during this state is crucial for prolonging battery life. This has made low power design a paramount consideration in CMOS circuit design. As we investigate into nanometer scales, power dissipation accounts for approximately 35% of chip power, potentially limiting chip functionality. This paper research into the major power dissipation mechanisms in digital logic circuits, emphasizing the exponential rise in sub-threshold leakage current due to reductions in the threshold voltage of MOS transistors. Various techniques to mitigate sub-threshold leakage, such as source biasing, stack technique, and multi-threshold CMOS (MTCMOS) technique, are discussed. Notably, while MTCMOS and super cutoff CMOS (SCCMOS) techniques are prevalent, they still exhibit considerable standby leakage power dissipation. This underscores the need for innovative circuit design techniques to further diminish standby leakage power consumption.
Keywords: Multi-threshold CMOS (MTCMOS), Super Cutoff CMOS (SCCMOS) Technique, CMOS Circuits

INTRODUCTION
With the persistent advancements in Very Large Scale Integration (VLSI) technology and the continual scaling down of supply and threshold voltages, the control of leakage has emerged as a pivotal factor in the power dissipation of modern Complementary Metal-Oxide-Semiconductor (CMOS) circuits. It is forecasted that, in the 90nm process generation, sub-threshold leakage power could account for approximately 42% of the total power, underscoring the significance of addressing leakage power consumption in Multi-threshold CMOS (MTCMOS) VLSI circuits.

The primary contributors to power dissipation in CMOS circuits, such as channel length, threshold voltage, and gate oxide thickness, are experiencing reductions, necessitating extensive research on optimizing the velocity and energy of these circuits. The goal is to achieve elevated speeds while maintaining minimal power consumptions. One of the prevalent methods to minimize the power consumption of digital circuits involves the reduction of the supply voltage. Moreover, the sub-threshold current, a principal leakage component in OFF devices, exhibits an exponential dependency on the supply voltage level, leading to a reduction in resistance.

The operational states of ON devices may vary, residing in super-threshold, near-threshold, or sub-threshold regions, depending on the extent of the supply voltage reduction. Operating in the sub-threshold region offers lower delays but incurs higher switching and leakage powers compared to near/sub-threshold regions. In this region, both the logic gate delay and leakage power demonstrate exponential dependencies on the supply and threshold voltages. These voltages are also subject to process and environmental variations in nanoscale technologies, increasing uncertainties in performance parameters and causing substantial delays for circuits operating in the sub-threshold region due to the minimal sub-threshold current.

The dependency of power and performance on the supply voltage has inspired the design of circuits with dynamic voltage and frequency scaling features. In such circuits, to conserve energy, the system can modify the circuit's voltage based on the workload requirement. The threshold voltage of transistors used in the design of digital circuits needs to be optimized to maximize savings in leakage power dissipation.

Several techniques, such as the MTCMOS technique, Super cutoff CMOS technique, Stack method, and Sleepy stack method, have been documented to control sub-threshold leakage power dissipation in deep submicron and nanoscale technologies. Each technique possesses its unique advantages and disadvantages, allowing chip designers to select the most suitable circuit design technique based on the requirements and applications. This paper introduces four novel digital circuit design techniques and applies them to a two-input AND gate to evaluate their performance. The findings indicate that the proposed techniques offer enhanced performance in terms of reduced sub-threshold leakage power dissipation in standby mode compared to other techniques documented in the literature.

Low power designs are coveted for their energy and temperature efficiency, extended battery life for portable devices, and reduced packaging and maintenance costs. MTCMOS technology employs high-speed, low Vt (LVT) transistors for logic cells and low leakage, high Vt (HVT) devices as sleep transistors to create an efficient power gating structure. However, MTCMOS circuits encounter several challenges, including long wakeup latency, substantial rush through current, and inefficient energy usage during mode transition. The major components of leakage power dissipation, such as sub-threshold leakage, gate leakage, gate induced drain leakage, and forward-biased diode leakage, are also explored in this article, providing a comprehensive overview of the complexities and innovations in leakage control in nanoscale MTCMOS VLSI circuits.

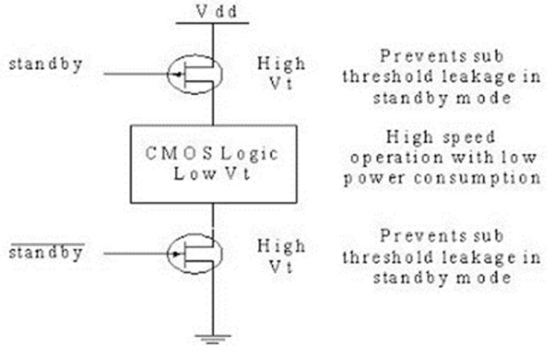
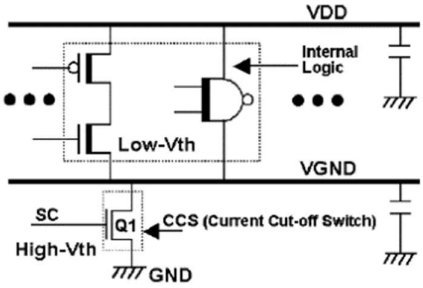


Figure 3.1: MTCMOS technique.

Preliminaries

The Principles of the MTCMOS: The MTCMOS circuit technology is proficient in attaining a reduced threshold voltage, leading to enhanced performance and diminished standby leakage current. Figure 3.2 depicts the fundamental circuit layout of MTCMOS.

Figure 3.2. Schematic Diagram of MTCMOS



The functional logic gates are constructed utilizing low Vth MOS transistors, which are powered by the supply line (VDD) and a virtual ground line (VGND). VGND is linked to the actual ground line (GND) via a high Vth MOS transistor switch, denoted as Q1. MTCMOS designs operate in two modes: active and sleep. In active mode, the Sleep Control (SC) signal is elevated, enabling the Q1 switch and establishing a direct connection between VGND and GND. As a result, the low Vth logic gates function regularly and with high speed. Conversely, in sleep mode, the SC signal is lowered, disabling Q1. In this condition, leakage current is directed to GND exclusively through the Q1 transistor. Given Q1's high Vth and its inherent low leakage, the leakage current originating from the low Vth logic gates is nearly entirely mitigated. Since Q1, the high Vth transistor, serves as a switch isolating leakage current from logic gates in sleep mode, it is termed the Current Cut-off Switch (CCS). Nonetheless, the activation resistance of the CCS can induce ground bounce in MTCMOS logic gates, potentially causing performance decline or failure. To counteract this ground bounce, the channel width of the CCS can be expanded. Regrettably, this expansion not only incurs area overhead but also augments the leakage current.

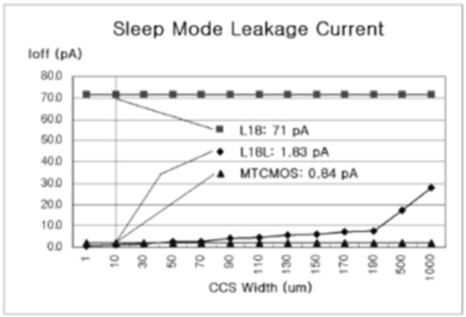


Figure 3.3 illustrates a comparison of sleep mode current in L18: Low Vth, L18L: High Vth, and MTCMOS: a combination of Low Vth + High Vth.

To evaluate the practicality of MTCMOS technology, we conducted SPICE simulations on an MTCMOS inverter, a low Vth inverter (L18), and a high Vth inverter (L18L), all implemented using 0.18µm technology. We set the leakage current of the high Vth inverter and the delay of the low Vth inverter as the lower bounds and measured the delay and leakage current of the

MTCMOS implementation, altering the width of the CCS in the process. The outcomes are represented in Figure 3.3.

An MTCMOS inverter, with an appropriately chosen CCS, attains a lower leakage current compared to the high Vth inverter while preserving the speed, ensuring it does not fall below that of the low Vth inverter. This decrement in leakage current can experience an exponential rise as the Vth is progressively reduced for additional performance augmentation.

MTCMOS Technique

In the active mode of the MTCMOS technique, high Vt transistors are deactivated, allowing the logic gates composed of low Vt transistors to function with reduced switching power dissipation and minimal propagation delay. Conversely, in standby mode, high Vt transistors are deactivated, isolating the internal low Vt circuitry.

Variable Threshold CMOS (VTCMOS)

VTCMOS is a proficient method to diminish power consumption by utilizing low supply and threshold voltages without compromising speed performance. However, the incorporation of devices with lower threshold voltages results in elevated sub-threshold leakage, leading to increased standby power consumption. VTCMOS devices, with their ability to vary the threshold voltage of low threshold devices by applying variable substrate bias voltage from control circuitry, offer a resolution to this issue.

VTCMOS is a highly effective technique to curtail power consumption, albeit with certain manufacturing-related drawbacks. It necessitates either twin well or triple well technology to facilitate different substrate bias voltage levels across various sections of the IC, with the area overhead of the substrate bias control circuitry being inconsequential.

Power Dissipation in Digital Logic Circuits

Power dissipation in digital logic circuits is predominantly categorized into dynamic power dissipation and static, or leakage, power dissipation. Dynamic power dissipation arises primarily from the current flow associated with the charging and discharging of parasitic capacitances within the logic circuit. Static power dissipation is prevalent during the device's static input states.

With advancements in technology leading to downscaling, the contribution of static power dissipation to overall power dissipation is escalating. In deep submicron CMOS technologies, sub-threshold leakage power dissipation is becoming the predominant factor among other leakage power components due to technological downscaling. In such scenarios, static power dissipation is nearly equivalent to sub-threshold leakage power dissipation and can be represented as:

$$P_{static} \approx P_{subthreshold}$$

A general formula for the total power dissipation in a digital logic circuit in deep submicron CMOS technologies can be expressed as

$$P_{total} = P_{dynamic} + P_{static}$$

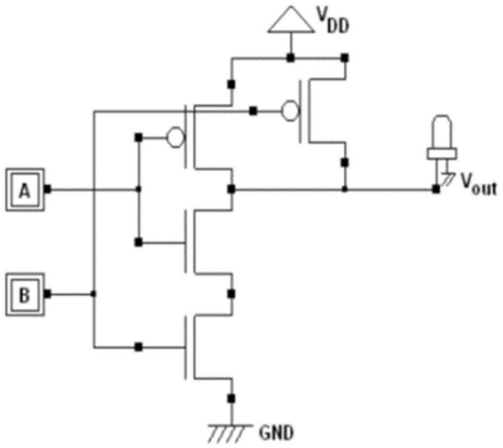
$$P_{total} = P_{dynamic} + P_{subthreshold}$$

CIRCUIT DESIGN USING VARIOUS TECHNIQUES

CONVENTIONAL CMOS TECHNIQUE

A traditional CMOS circuit is composed of two main networks: a pull-up network and a pull-down network. The pull-up network is formed of pMOS transistors, and the pull-down network is comprised of nMOS transistors. In employing this method, every pMOS transistor should receive an input either from the power supply voltage (VDD) or from another pMOS transistor. In a similar fashion, each nMOS transistor should be connected to either ground or another nMOS transistor. Figure 3.3.1 illustrates the schematic representation of a two-input NAND gate constructed using this methodology.

Fig. 3.3.1 Circuit diagram of a two input NAND gate using conventional CMOS technique.



STACK TECHNIQUE

In the stack technique, a MOS transistor with a width of W is substituted by two MOS transistors connected in series, each having a width of W/2. Figure 3.3.2 depicts the circuit diagram of a two-input NAND gate utilizing this method. In this illustration, every MOS transistor (with a width of W) in a CMOS two-input NAND gate is replaced by two MOS transistors connected in series (each with a width of W/2). When both half-sized stacked MOS transistors are simultaneously turned off, it induces a reverse bias between them, leading to a reduction in sub-threshold leakage power. However, the addition of more transistors augments the overall propagation delay of the circuit.

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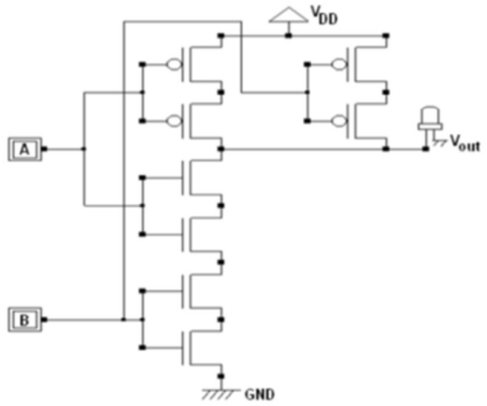
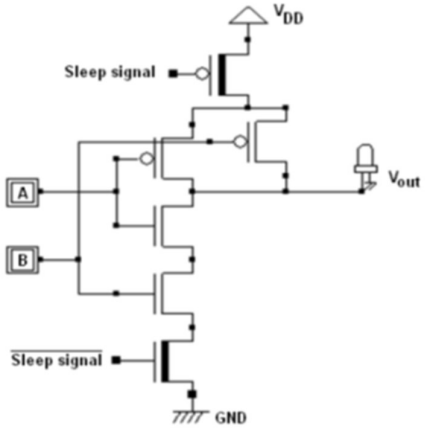


Fig. 3.3.2 Circuit diagram of a two input NAND gate using stack technique.

Overview of MTCMOS TECHNIQUE

In the MTCMOS approach (as described by Mutoh et al. in 1995), a pMOS transistor with a high threshold voltage (referred to as the sleep pMOS transistor) is positioned between the power supply voltage (VDD) and the logic circuit. Simultaneously, an nMOS transistor with a high threshold voltage (termed the sleep nMOS transistor) is connected between the logic circuit and the ground. Figure 3.3.3 illustrates the circuit design of a two-input NAND gate employing this method. When the system is in active mode, the high threshold voltage MOS transistors (also known as sleep transistors) are activated. Conversely, in sleep mode, these high VTH transistors are deactivated.

Fig. 3.3.3 Circuit diagram of a two input NAND gate using MTCMOS technique



The Hybrid MTCMOS Stack Technique is a proposed method that blends the benefits of both MTCMOS and Stack techniques to optimize power consumption in integrated circuits. It is primarily categorized into:

- **Hybrid MTCMOS Complete Stack Technique**
- **Hybrid MTCMOS Partial Stack Technique**

These techniques aim to enhance performance by reducing leakage power compared to other methods.

Multi-threshold CMOS (MTCMOS):

MTCMOS is a variant of CMOS technology, utilizing transistors with varying threshold voltages to balance delay and power. Transistors with low threshold voltages switch faster, benefiting critical delay paths, but have higher static leakage power. Conversely, high threshold voltage transistors, used in non-critical paths, minimize static leakage power without compromising delay.

MTCMOS:

MTCMOS is created by adjusting the threshold voltages of transistors during the fabrication process. This is achieved by altering the dopant concentration in the channel region beneath the gate oxide, typically using ion implantation methods, and involves additional photolithography and ion implantation steps.

Hybrid MTCMOS Complete Stack Technique:

This technique inserts a high threshold voltage PMOS transistor between the power supply (VDD) and the logic circuit, and a high threshold voltage NMOS transistor between the logic circuit and the ground (GND). Further, all transistors are stacked by replacing each transistor of width W with two series-connected transistors, each of width W/2.

The Hybrid MTCMOS Stack Techniques are advantageous as they combine the strengths of MTCMOS and Stack techniques, offering improved performance in terms of reduced leakage power. This technique as a smart power-saving mode in electronic circuits. It uses different types of switches (transistors) that are either fast but power-consuming or slow but power-saving. By smartly combining these switches in a stack formation, it manages to save power without compromising much on performance.

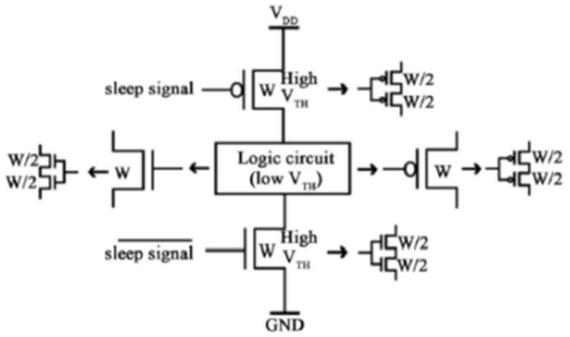


Figure 3.4. Logic circuit using hybrid MTCMOS complete stack technique.

Standby Mode:

In standby mode, a sleep signal is activated, causing the high threshold voltage (VTH) pMOS and nMOS transistors to cut off. This disconnects the logic circuit from the power supply (VDD) and ground (GND), significantly reducing power leakage due to the utilization of these cut-off transistors. When the system is active or in normal mode, these high VTH transistors are turned on.

Implementation:

MTCMOS is commonly implemented to reduce power using sleep transistors. These transistors connect the actual and virtual power rails, using low VTH devices in the logic for fast switching and high VTH devices as sleep transistors to minimize power leakage. The design of the power switch, which controls the power supply to the logic gates, is crucial as it influences the speed, area, and power of a logic circuit.

Coarse-Grained Approach:

In this approach, high VTH sleep transistors control power to entire logic blocks. These transistors are large and must be carefully sized to supply the required current by the circuit block. This method involves partitioning logic blocks and adding an always-active power management circuit, which are considered as drawbacks.

Fine-Grained Approach:

Here, high VTH sleep transistors are included within every gate, eliminating the problems of logic block partitioning and sleep transistor sizing. However, this approach incurs a large amount of area overhead due to the inclusion of additional transistors in every Boolean gate and the creation of a sleep signal distribution tree.

Intermediate Approach:

This approach incorporates high VTH sleep transistors into threshold gates with more complicated functions, requiring less area overhead. This method is seen in Null Convention Logic and Sleep Convention Logic.

Hybrid MTCMOS Partial Stack Technique:

In this technique, a high VTH pMOS transistor is placed between VDD and the logic circuit, and a high VTH nMOS transistor is placed between the logic circuit and GND. Only the high VTH pMOS and high VTH nMOS transistors are stacked. The low VTH MOS transistors of the logic circuit are not stacked in this technique.

The system as having a sleep mode and an active mode. In sleep mode, certain components (transistors) are turned off to save power, and in active mode, they are turned on to perform tasks quickly. Different approaches are used to implement this system, each with its own advantages and disadvantages, affecting the overall efficiency and area of the logic circuit. The Hybrid MTCMOS Partial Stack Technique is a specific method where only certain components are stacked to balance power consumption and performance.

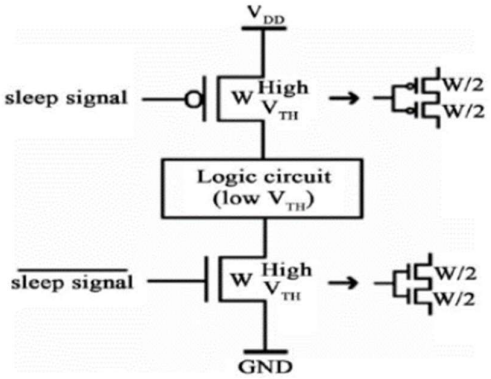


Fig 3.5 Logic circuit using hybrid MTCMOS partial stack technique.

Hybrid MTCMOS Partial Stack Technique:

In this method, only high VTH pMOS and high VTH nMOS transistors are partially stacked to minimize the circuit propagation delay during active mode. In standby mode, these stacked transistors are turned off, significantly reducing sub-threshold leakage power dissipation. This technique slightly reduces circuit propagation delay in active mode compared to the complete stack technique due to the partial stacking of transistors.

Analysis of CMOS Leakage Power Supply:

Leakage:

Leakage refers to the unintentional transfer of electrical energy across supposed insulating boundaries. It can occur in various components like capacitors, between electronic assemblies, and in semiconductors.

In Capacitors

Leakage in capacitors is mainly due to attached electronic devices and imperfections in dielectric materials, causing a slow discharge of the capacitor. It can also occur when current leaks out of the intended circuit, potentially causing damage, fires, or electrocution.

Between Electronic Assemblies and Circuits:

Leakage can mean the unwanted transfer of energy from one circuit to another, causing issues like audible hum in audio applications. It is also significant in standby or "sleep" mode in electronic assemblies, affecting battery run time in portable devices.

In Semiconductors:

Leakage in semiconductors is a quantum phenomenon where charge carriers tunnel through an insulating region, increasing exponentially as the thickness of the insulating region decreases. It is one of the main factors limiting increased computer processor performance. Efforts to minimize leakage include the use of new materials and proper system design. Increased leakage can indicate manufacturing defects or non-catastrophic overstress of a semiconductor device.

Leakage Current Mechanisms:

Leakage current, generally measured in microamperes, is temperature-sensitive and must be carefully examined in applications working in wide temperature ranges. In nanometer devices, it is dominated by sub-threshold leakage, gate-oxide tunneling leakage, and reverse-bias pn-junction leakage.

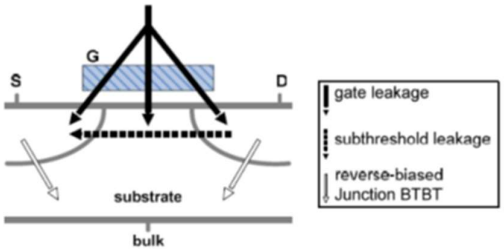


Fig. 4.2. Major leakage mechanisms in MOS transistor

Sub-threshold Current

Sub-threshold Current:

To control dynamic power consumption, supply voltage is reduced. To maintain high drive current capability in this scenario, the threshold voltage (Vth) also needs to be reduced. However, reducing Vth leads to an increase in sub-threshold leakage currents.

Sub-threshold current happens when a transistor is in a weak inversion region, meaning the gate voltage is less than Vth. This occurs between the drain and the source of the transistor.

When the transistor is in strong inversion, meaning the gate-to-source voltage is more than Vth, the drain-to-source current is mainly composed of drift current. However, in weak inversion, the channel has no horizontal electric field, and carriers move by diffusion between the source and the drain of the MOS transistor. In this state, the sub-threshold current is primarily due to diffusion current and is exponentially dependent on both gate-to-source and threshold voltage. Considering the BSIM MOS transistor model, the sub-threshold leakage current for a MOSFET device can be expressed as:

$$I_{Subthreshold} = I_o e^{\frac{V_{GS}-th}{nV_T}} \left(1 - e^{\frac{-V_{dS}}{V_T}}\right) \quad (4.1)$$

Where $I_o = \mu C_{ox} \frac{W}{L} {V_T}^2 e^{1.8}$ And $V_T = \frac{KT}{q}$ are the thermal voltage, Vth is the threshold voltage, Vds and Vgs are the drain-to-source and gate-to-source voltages respectively. W and L are the effective transistor width and length, respectively. Cox is the gate oxide capacitance, μ0 is the carrier mobility and n is the sub-threshold swing coefficient.

Short Channel Effects (SCE) in Devices:

In devices with short channels, the depletion regions of the source and drain significantly encroach into the channel, altering the internal field and potential profile, known as short channel effects (SCE). These effects lower the transistor threshold voltage due to the reduction

in channel length (Vth roll-off) and the increase in Drain Induced Barrier Lowering (DIBL). Consequently, substantial sub-threshold current occurs in short channel devices.

Gate Oxide Tunneling Current:

With aggressive device scaling in the nanometer regime, short channel effects like DIBL and Vth roll-off intensify. To manage these effects, the oxide thickness also needs to be reduced progressively. However, reducing oxide thickness leads to high electric fields and, subsequently, high direct-tunneling current through the transistor gate insulator.

Gate oxide tunneling current refers to the tunneling of electrons or holes through the gate oxide potential barrier into the gate, associated with the MOS capacitance concept. There are three major gate leakage mechanisms in a MOS structure:

- **Electron Conduction-**Band Tunneling (ECB): Electrons tunnel from the conduction band of the substrate to the conduction band of the gate.
- **Electron Valence-**Band Tunneling (EVB): Electrons tunnel from the valence band of the substrate to the conduct band of the gate.
- **Hole Valence-**Band (HVB) Tunneling: Holes tunnel from the valence band of the substrate to the valence band of the gate.

These mechanisms are illustrated in Fig. 4.3, showcasing the different pathways through which electrons or holes can tunnel, contributing to the overall gate oxide tunneling current.

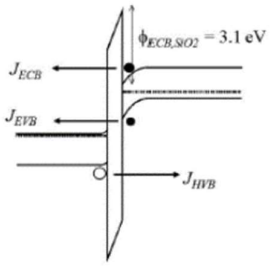


Fig. 4.3. Three mechanisms of gate dielectric direct tunneling leakage.

Each mechanism is dominant or important in different regions of operation for NMOS and PMOS transistors. For each mechanism, gate leakage current can be modeled by:

$$I_{gate} = W.L.A\left(\frac{V_{ox}}{t_{ox}}\right)^2 exp^{\left[\frac{-B\left[1-\left[1-\frac{V_{ox}}{\emptyset_{ox}}\right]^{3/2}\right]}{\frac{V_{ox}}{t_{ox}}}\right]} \quad (4.2)$$

Where W and L are the effective transistor width and length, respectively, $A = {q^3}/{16\pi^2 h\emptyset_{ox}}$, $B = {4\pi\sqrt{2m_{ox}}\emptyset_{ox}}^{3/2}/{3h\,q}$ is the effective mass of the tunneling particle, $\emptyset_{ox}$ is the tunneling barrier height, t_{ox} is the oxide thickness, h is 1/2π times Planck's constant and q is the electron charge.

Band-to-Band Tunneling Current

The MOS transistor is characterized by the presence of two pn junctions, specifically the drain and source to well junctions. Typically, these junctions are in a state of reverse bias, leading to

the manifestation of a leakage current associated with the pn junction. The magnitude of this current is determined by factors such as the junction area and the concentration of doping.
In scenarios where the 'n' and 'p' regions undergo heavy doping, the leakage mechanism of the reverse-biased pn junction is predominantly governed by band-to-band tunneling (BTBT) leakage. This phenomenon occurs due to the existence of a high electric field across the reverse-biased pn junction, facilitating a current flow through the junction. This is attributed to the tunneling of electrons from the valence band situated in the p-region to the conduction band of the n-region, a process illustrated in Fig. 4.4.

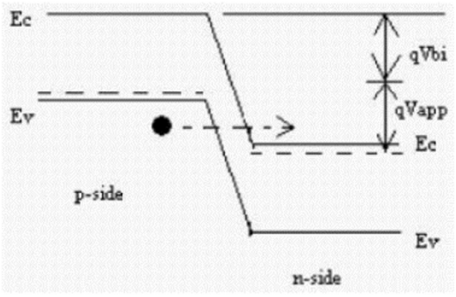


Fig. 4.4. BTBT in reverse-biased pn junction.

Tunneling current occurs when the total voltage drops across the junction, applied reverse bias (Vapp) plus built-in voltage (ψbi), is larger than the band-gap. The tunneling current density through a silicon pn junction is given by:

$$J_{BTBT} = A \frac{EV_{app}}{E_g^{1/2}} exp\left[-B \frac{E_g^{3/2}}{E}\right] \quad (4.3)$$

Where $A = \sqrt{2m^*}q^3/4\pi^3h^2$ and $B = 4\sqrt{2m^*}/3h\ q\ .\ m^*$ are the effective mass of electron; Eg is the energy-band gap; Vapp is the applied reverse bias; E is the electric field at the junction; q is the electron charge; and h is 1/2π times the Planck's constant.

In contemporary processes, band-to-band tunneling leakage is often deemed negligible, especially when juxtaposed with sub-threshold and gate oxide leakages. However, this form of leakage begins to gain relevance in technologies that operate at 25nm scales. The current that tunnels through the junction is exponentially dependent on both the doping within the junction and the extent of reverse bias applied across it. Employing forward body bias serves as a viable strategy to mitigate the leakage caused by band-to-band tunneling.

RESULTS AND DISCUSSION

SIMULATION RESULTS

Figs. 5.1 – 5.6 show the layout diagrams of a two input NAND gate and a one-bit ALU using existing techniques (MTCMOS) and proposed techniques (hybrid MTCMOS complete stack technique, hybrid MTCMOS partial stack technique.

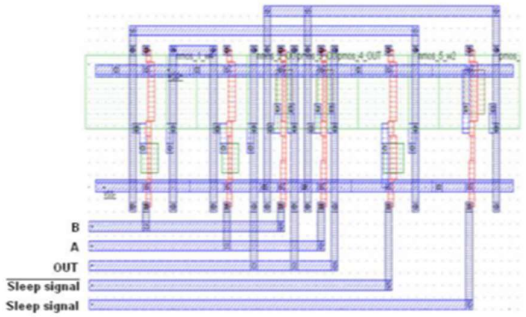


Fig. 5.1 Layout of a two input NAND gate using MTCMOS technique.

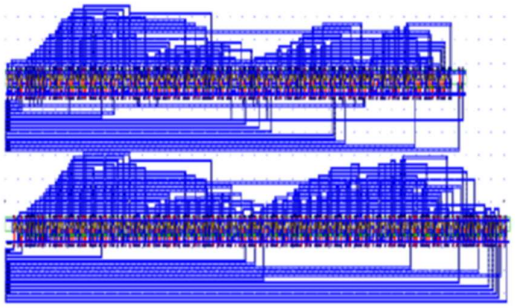


Fig. 5.2 Layout of a one-bit ALU using MTCMOS technique.

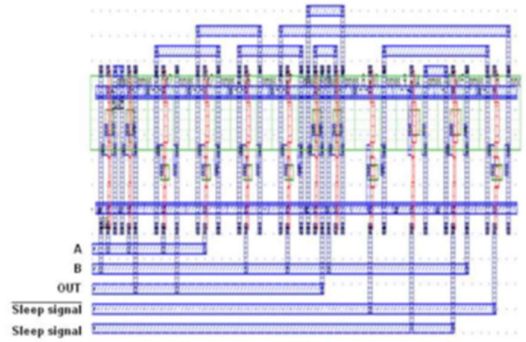


Fig. 5.3 Layout of a two input NAND gate using hybrid MTCMOS complete stack technique.

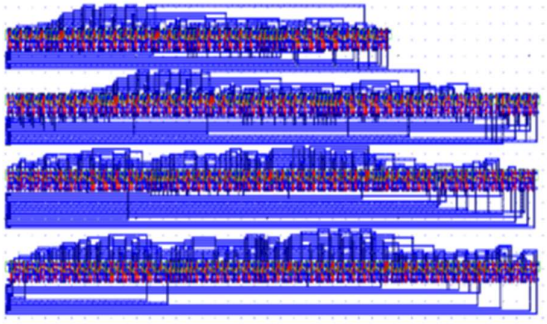


Fig. 5.4 Layout of a one-bit ALU using hybrid MTCMOS complete stack technique.

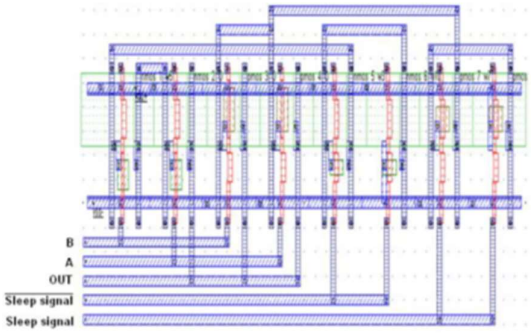


Fig. 5.5 Layout of a two input NAND gate using hybrid MTCMOS partial stack technique

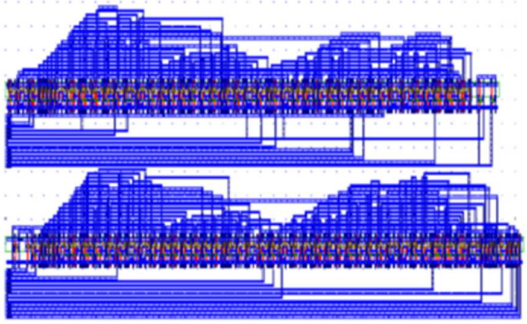


Fig. 5.6 Layout of a one-bit ALU using hybrid MTCMOS partial stack technique

The proposed circuit technique's efficacy, utilizing SOI CMOS technology, is evaluated against existing MTCMOS and SCCMOS techniques in both CMOS bulk and SOI CMOS technologies, focusing on the dissipation of standby sub-threshold leakage power. A one-bit full adder serves as the basis for this comparative analysis.

Tables 5.1 – 5.2 present performance metrics, including sub-threshold leakage power dissipation in standby mode and propagation delay, for a two-input NAND gate and a one-bit ALU, employing both existing and the proposed circuit techniques. Subsequently, Tables 5.3 – 5.4 provide insights into the standby sub-threshold leakage power reduction factors for a two-input NAND gate and a one-bit ALU, showcasing the enhancements brought about by the improved SOI CMOS technology-based circuit technique in relation to other existing and proposed methodologies.

Table 5.1: Performance characteristics of a two input NAND gate using proposed and existing circuit techniques

Techniques	**Technology**	**Standby sub-threshold power (in nW)**	**Delay (in sec.)**
MTCMOS technique	120nm CMOS	0.0385	16.21×10^{-12}
Hybrid MTCMOS complete stack technique	120nm CMOS	0.0159	25.4×10^{-12}

Hybrid MTCMOS partial stack technique	120nm CMOS	0.017	22.8 x 10^{-12}

Table 5.2: Performance characteristics of a one-bit ALU using proposed and existing circuit techniques

Techniques	Technology	Standby sub-threshold power (in nW)	Delay (in sec.)
MTCMOS technique	120nm CMOS	3.75	1.48 x 10^{-9}
Hybrid MTCMOS complete stack technique	120nm CMOS	1.51	2.39 x 10^{-9}
Hybrid MTCMOS partial stack technique	120nm CMOS	1.71	1.97 x 10^{-9}

Table 5.3: Comparison of Standby Sub-threshold Leakage Power Reduction Factors for a Two-Input NAND Gate Using Proposed and Existing Techniques

Techniques	Standby sub-threshold leakage reduction factor
MTCMOS technique	38x
Hybrid MTCMOS complete stack technique	15x
Hybrid MTCMOS partial stack technique	17x

Table 5.4: Comparison of Standby Sub-threshold Leakage Power Reduction Factors for a One-Bit ALU Using Proposed and Existing CMOS Technology-Based Techniques

Techniques	Standby sub-threshold leakage reduction factor
MTCMOS technique	37.5x
Hybrid MTCMOS complete stack technique	15.1x
Hybrid MTCMOS partial stack technique	17.1x

The measurement of standby sub-threshold leakage power dissipation involves considering all possible static input combinations, ensuring the voltage magnitude of the inputs remains below the threshold voltage of the low VTH MOS transistors in a two-input NAND gate. This dissipation is assessed over a 50ns interval using both existing and proposed methodologies.The propagation delay of a logic gate is determined from the point where the input edge triggers 50% of VDD to the moment the circuit output edge reaches 50% of VDD. A one-bit full adder circuit layout was designed and simulated utilizing the Micro wind ver. 3.1 EDA tool. All simulations were conducted at 27˚C with a supply voltage, VDD, of 0.9 V in 120 nm SOI CMOS and bulk CMOS technologies. The W/L of low VTHnMOS and pMOS transistors were designated as 0.72 μm/0.12 μm and 1.20 μm/0.12 μm respectively, and the

W/L of high VTHnMOS and pMOS transistors were 0.72 μm/0.24 μm and 1.20 μm/0.24 μm respectively.

The standby sub-threshold leakage power dissipation was measured by integrating all possible input vector combinations, ensuring the voltage magnitude of all input vectors is consistently below the threshold voltage of the MOS transistor in the logic circuit. In the proposed technique, the sub-threshold leakage power dissipation in standby mode for a one-bit full adder was computed by connecting reverse gate voltages, VGS1 and VGS2, to high VTH stacked MOS transistors and applying all combinations of static input voltages, Vin < VTH, to the logic circuit. Dynamic power dissipation was calculated by applying input clock signals at a frequency of 5 GHz using this proposed technique.

Tables 5.5 and 5.6 respectively display the standby sub-threshold leakage power dissipation and the standby sub-threshold leakage reduction factor for a one-bit full adder circuit using the proposed technique in SOI CMOS technology, compared with existing techniques in CMOS bulk technology.

Techniques	Standby sub-threshold leakage power dissipation	Dynamic power dissipation
MTCMOS	0.049nW	0.045μW

Table 5.6. Standby sub-threshold leakage reduction factor and dynamic power dissipation reduction factor using the proposed technique in SOI CMOS technology in comparison with other existing techniques in CMOS bulk technology.

Techniques	Standby sub-threshold leakage power dissipation	Standby sub-threshold leakage reduction factor for the proposed technique in comparison to the existing technique
Multi-threshold	0.010 nW	10x

CONCLUSION

Reducing sub-threshold leakage power in standby mode is crucial for burst mode circuits, which are predominantly in standby mode and only active during brief computational intervals. The unnecessary depletion of battery power during extended standby phases is particularly detrimental in portable devices like cell phones and pagers, which operate in active mode for minimal durations and expend battery power predominantly during prolonged standby periods. This is also applicable to portable laptops, where battery leakage in standby mode is undesirable. Implementing sub-threshold leakage reduction techniques during standby can notably mitigate leakage in such applications.

This paper introduces the transition of standby sub-threshold leakage control techniques from bulk CMOS to SOI CMOS technology. It proposes an enhanced SOI CMOS technology-based

circuit technique aimed at efficiently minimizing standby sub-threshold leakage power dissipation. The effectiveness of the proposed technique is substantiated through the layout design and simulation of a one-bit full adder circuit, comparing it with other existing leakage control techniques.

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