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IMPLEMENTATION OF PARALLEL COMPUTING AND ADIABATIC LOGIC IN FULL ADDER DESIGN FOR ULTRA LOW POWER APPLICATIONS

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Abstract :
This paper describes three different designs of a full adder based on adiabatic logic. The first design (A-I) uses parallel computing to reduce the delay time, while the second design (A-II) uses two-phase clocked adiabatic static complementary metal oxide logic to decrease power dissipation. The third design (A-III) uses parallel computing for both sum and carry generation and introduces a buffer to restore the logic level. The results of the designs are compared to previous approaches, and it is found that A-II and A-III show significant improvements in power delay product (PDP) compared to other designs. Additionally, the designs perform well under varied temperature conditions and are energy-efficient for low power applications. Overall, the proposed designs show promise for improving the performance and energy efficiency of full adders, particularly for low power applications. The use of adiabatic logic and parallel computing techniques are effective in reducing delay time and power dissipation, respectively.
Keywords : Adiabatic logic · Energy efficiency · Low power adder · Parallel computing · Power delay product

INTRODUCTION:

Energy efficiency with high speed in low-power ultralarge-scale integrated circuits has attracted the attention of researchers in the nanometer regime according to [1], as this is the prime need for modern electronic devices to prolong the battery life. The feature size of metal oxide semiconductor devices is improving (miniaturization) day by day consequently. With improved scaling in deep sub-micrometer regime, leakage current is becoming considerable,

as it contributes a sizable fraction to the total power dissipation of a chip mentioned in [2]. The lowpower electronic industry is progressing by leaps and bounds with the high demand for portable electronic devices. These devices consist of high-speed data processors that perform complex operations employing MOS as fundamental blocks. Large-scale industrial automation, space applications, image processing, modern warfare industry, biomedical implantable devices, and other modern miniaturized electronic devices consist of digital signal processing (DSP) units [3]. These units are used to perform arithmetic and logical operations utilizing multiplier and high-speed adders. Therefore, the selection of adder topologies becomes the prime concern for the designer to make the system energy efcient with high speed, particularly in multipliers. Various increasing limitations of decreasing nanometer technologies have attracted the researcher's attention to the search for new hybrid circuits and techniques for electronic devices. The adiabatic logic technique is one of the prominent techniques of power reduction [4]. In the literature, various techniques have been reported which are used to implement the adders for modern electronic systems. Some have limitations of the area, and some other has limitations of delay, capacitance, and swing in output voltage [5]. Conventional static CMOS-based circuits occupy a large area of the chip and increased leakage currents with improved scaling. A hybrid adder based on complementary pass transistor (CPL) logic has been reported in [6]. In this circuit, the frst part consists of X-OR/ X-NOR which consists of NMOS with one inverter. Reduced delay in this circuit is advantageous, but it dissipates more power as in [7] and [8]. An approximate 4–2 compressor circuit has been reported in [9] which reduces the number of adders required, but approximate compressors are erroneous. A fourth passive element memristor-based adder has been presented in [10] with some constraints such as commercial availability and speed as compared to MOS devices. Another hybrid full adder with a strong driver and good voltage swing has been reported in [11]. However, the functioning of hybrid adders requires less power, but their decreased speed and increased number of transistors become a constraint for high-frequency computations [7]. In this paper, the novelty of these new proposed designs of full adder circuits is based on parallel computing. These adders compute the sum parallelly which results in very high speed with reduced power dissipation. In A-I, carry is separately computed with three transistors-based X-OR gate [12] and multiplexer (MUX). In the second design A-II, two-phase clocked adiabatic static CMOS logic (2PASCL) [13] has been used, whereas A-III computes carry and sum both parallel.

2.Fundamental concepts and related terminologies

2.1 Mechanism of power dissipation in a CMOS

the mechanism of power dissipation in a CMOS device, which is responsible for draining the battery and affecting the performance of the device. There are three dominant sources of power dissipation in a MOS device, including dynamic power dissipation, short circuit power dissipation, and static power dissipation. The total power dissipation in a MOS device is a combination of these three components. Dynamic power dissipation occurs when charging and discharging of capacitances during switching of the transistor states, short circuit power dissipation occurs when both the NMOS and PMOS are conducting simultaneously, and static power dissipation occurs due to leakage currents in the off-state. The understanding of these power dissipation mechanisms is crucial for the design of low-power electronic devices.

• Dynamic power dissipation
• Short circuit power dissipation
• Static power dissipation.

PT = PD + PSC + PS

where PT is the total power dissipation of a MOS device.

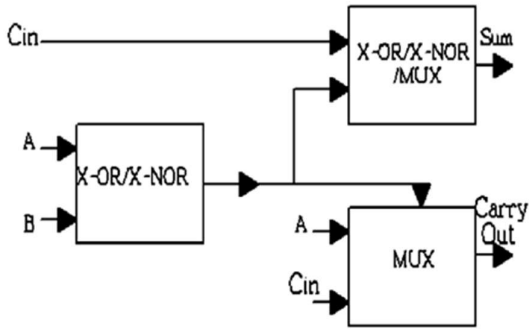


Fig 1 Basic structure of full adder

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 1 Truth Table of full adder

2.2 Logical composition of full adder

the architecture of a full adder consists of three blocks: the first block contains XOR/XNOR gates, the second block contains XOR/XNOR gates and a multiplexer, and the third block contains a MUX for carry generation. The three inputs to a full adder are A, B, and Cin (carry-in), and it produces two outputs, sum and carry-out.

The truth table for a full adder with all possible input combinations of A, B, and Cin and their corresponding sum and carry-out values is given in Table 1.

The basic functionality of a full adder can be expressed using the following equations:

Sum = A XOR B XOR Cin

Carry-out = (A AND B) OR (Cin AND (A XOR B))

2.2 ADIABATIC LOGIC

The term “Adiabatic” has been taken by thermodynamic means no energy transfer to the environment, so there is no dissipated energy loss. In real-life computing, because of the presence of dissipative elements like resistance in a circuit ideal process cannot be achieved. However, low energy dissipation can be achieved by slowing down the speed of operation and only switching transistor under certain conditions. Adiabatic circuits are low power circuits which need ‘reversible logic’ to conserve energy [1].

A. Operation of Adiabatic Logic

Adiabatic offers a way to reuse the energy stored in the load capacitor, rather than discharging the load capacitor to the ground and wasting this energy. Operations of adiabatic logic circuits are based on some basic rules such as never turn on a transistor when there is a voltage potential between the source and drain terminals, and never suddenly change the voltage across any of the transistor [7]. The adiabatic logic is broadly known as ENERGY RECOVERY CMOS logic as it uses reversible logic to conserve energy. Adiabatic logic families can be classified as:- Partially Adiabatic:- In partially adiabatic or Quasi adiabatic circuits, some charge gets transferred to the ground i.e. some heat is dissipated. Hence a part of the energy is only being able to recover, but these circuits are easy to implement as compared to fully adiabatic logic circuits.

Some partially adiabatic logic families are:-

1. Efficient Charge Recovery Logic (ECRL)
2. 2N-2N2P Adiabatic Logic
3. Positive Feedback Adiabatic Logic (PFAL)
4. Clocked Adiabatic Logic

Fully Adiabatic:-

In fully adiabatic circuits, all the charges on the load capacitance gets recovered and feedback to the power supply. Due to which fully adiabatic circuits become slower and complex as compared to partial adiabatic circuits .

Some fully adiabatic logic families are:-

1. Pass Transistor Adiabatic Logic (PAL)
2. Two Phase Adiabatic Static CMOS Logic (2PASCAL)
3. Split-Rail Charge Recovery Logic (SCRL)

B. Adiabatic Switching:

An adiabatic switching is an alternative solution to reduce power dissipation in the digital logic. The energy stored in the output gets retrieved by reversing the current source direction. Fig. 1. Adiabatic Switching Circuit. Here, the constant current source is used to charge the load capacitance not a constant voltage source as used in the

case of conventional CMOS circuits. Where, R represents the onresistance of PMOS network. The constant current power supply is capable of retrieving the energy back from the circuit. Thus, adiabatic logic circuits require non-standard power supplies with time varying voltages such as pulsed power supplies. Assume, that the capacitor voltage vc is zero initially,

the voltage over the switch =IR P(t) in the switch = I2R

Energy during charge = (I2R)T

$E = (I2R)T = C2V2/TR$-- (1)

$E = (RC/T)\ CV2 = (2RC/T)\ (1/2C)$-- (2)

Here, E = dissipated energy during charging,

Q = charge transfer to the load,

C = load capacitance value,

R = on- resistance of PMOS switch,

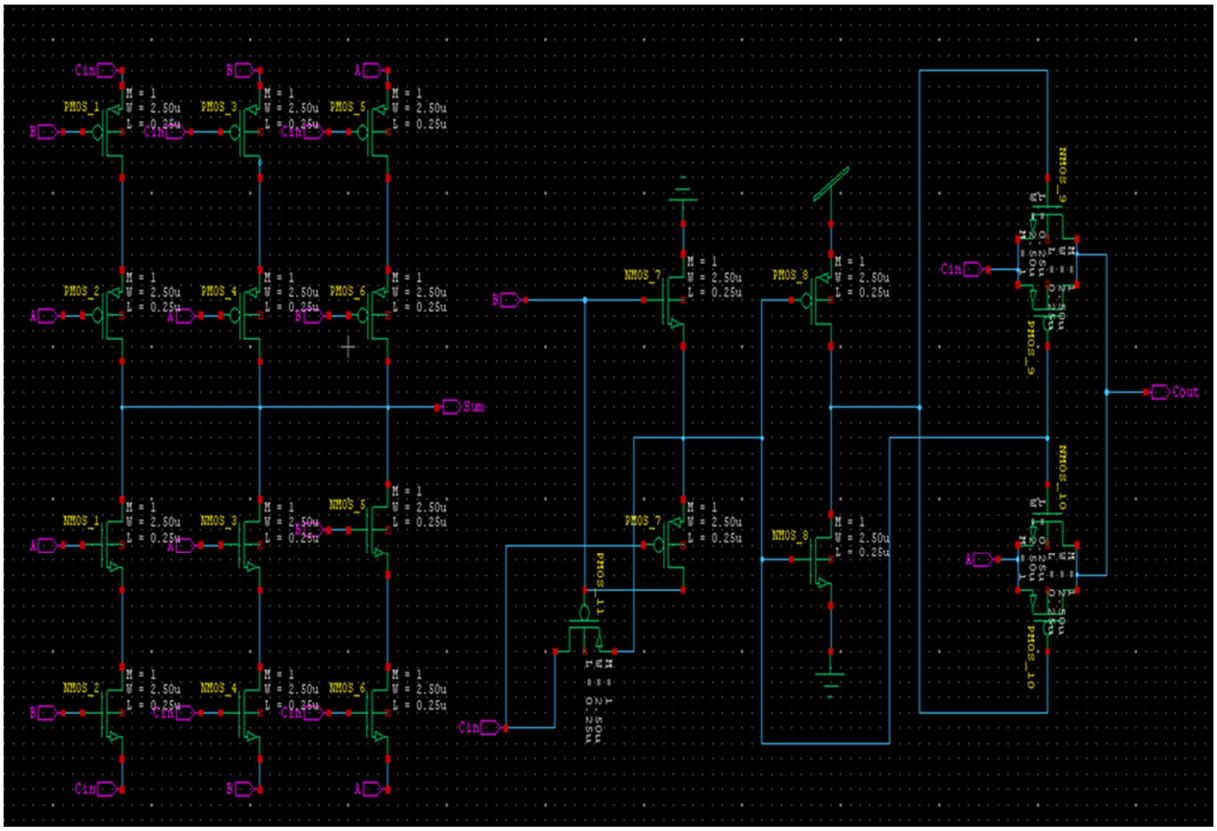
V = voltage final value at load,

T = charging time. Hence,

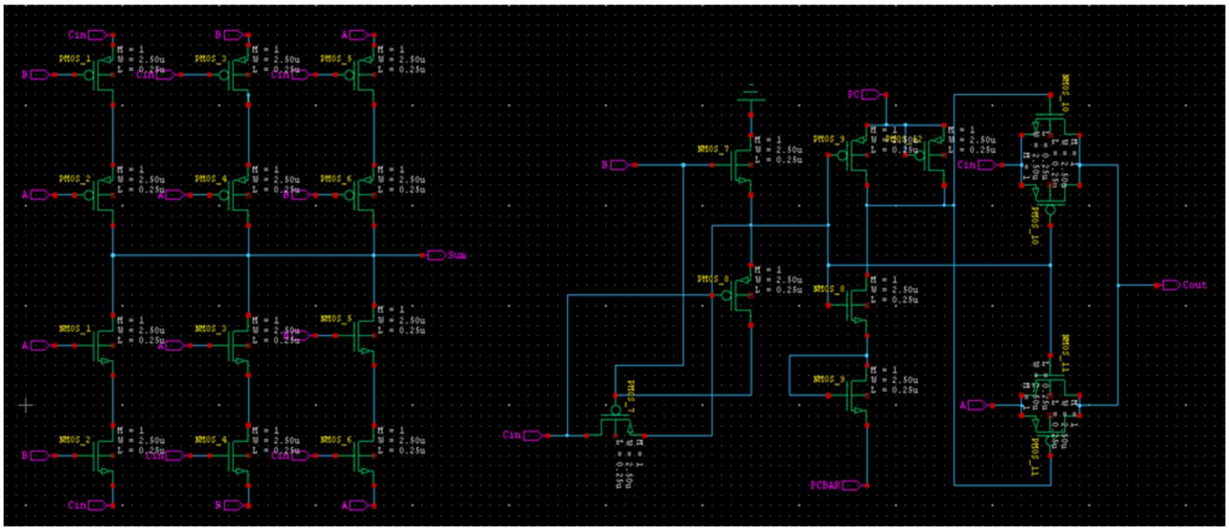
the dissipated energy can be reduced by reducing the on-resistance of PMOS network and increasing the charging time.

3. CIRCUIT IMPLEMENTATION

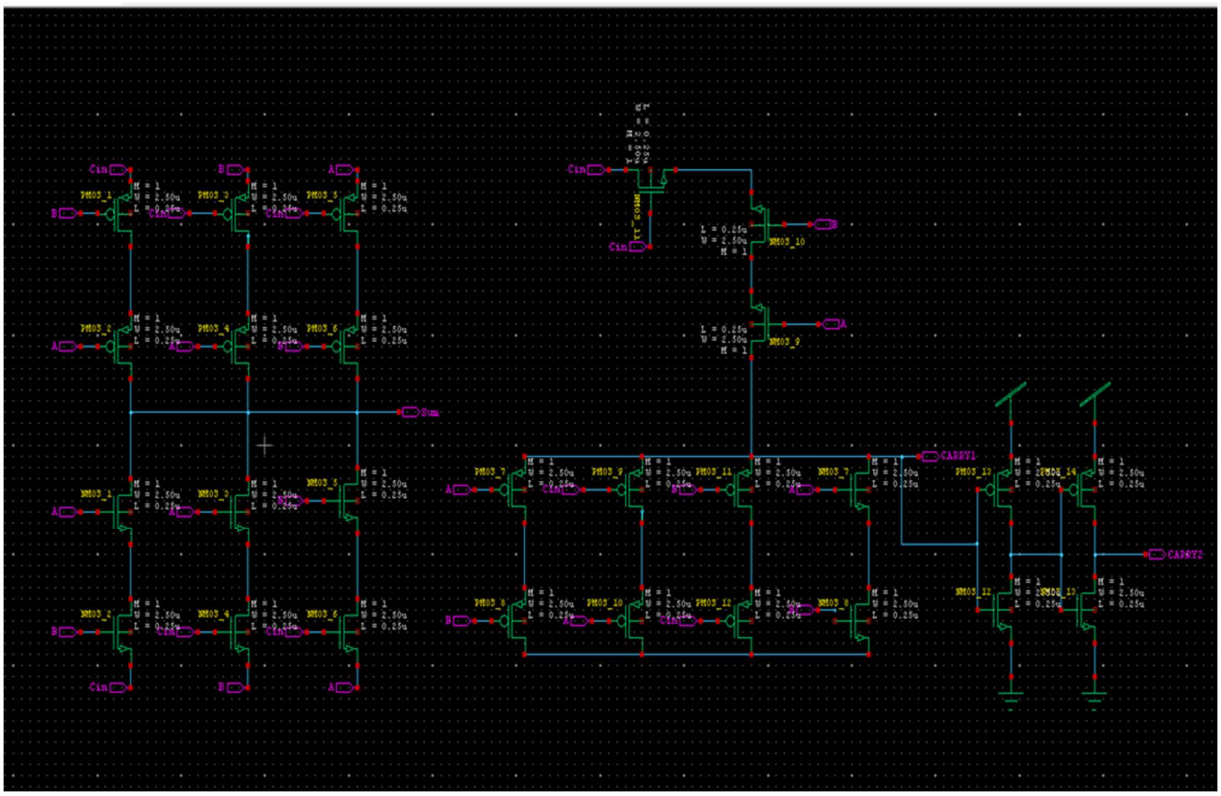
3.1 : DESIGN AND IMPLEMENTATION Proposed OF FULL ADDER-1



3.2:DESIGN AND IMPLEMENTATION Proposed OF FULL ADDER-2



3.3 : DESIGN AND IMPLEMENTATION Proposed OF FULL ADDER-3



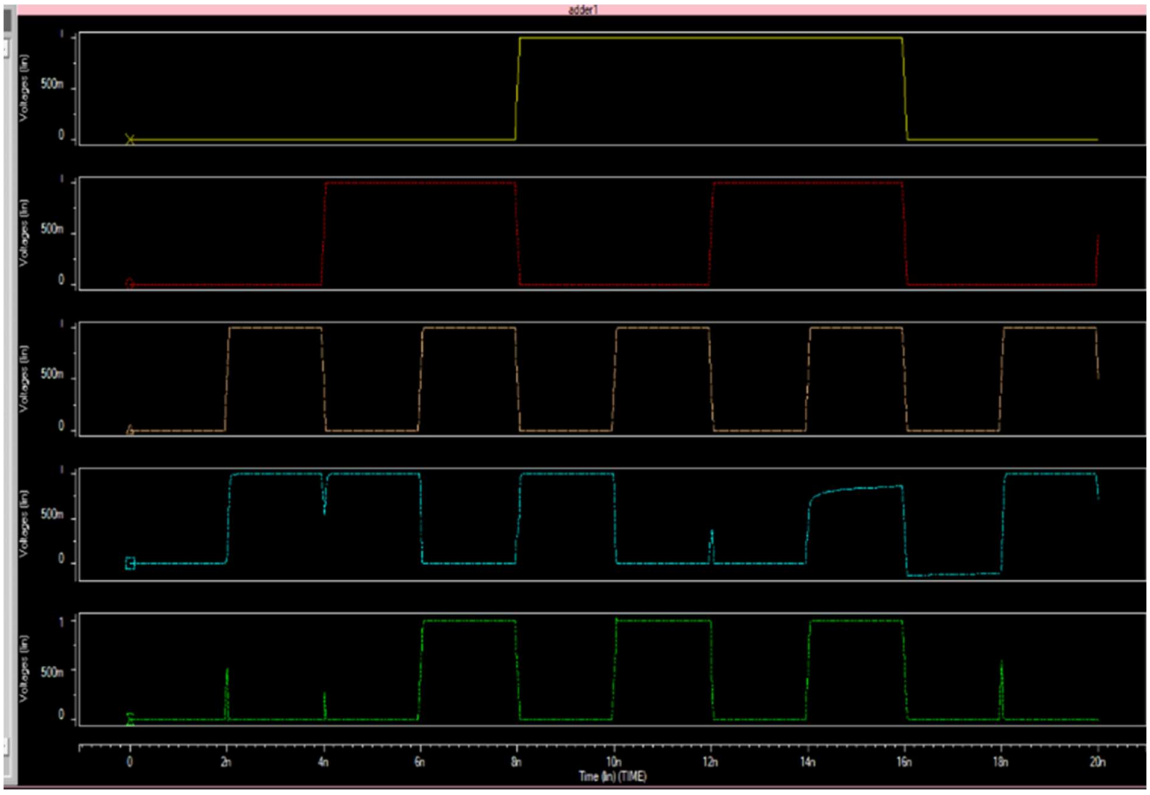
A. Cmos Specifications

specifications	Values
Technology	90nm
Power Supply	0.9v
PMOS Transistor width	440nm
PMOS transistor length	90nm
NMOS transistor width	220nm
NMOS transistor length	90nm
Period of pulse	40ns
Rise time	10ps
Fall time	10

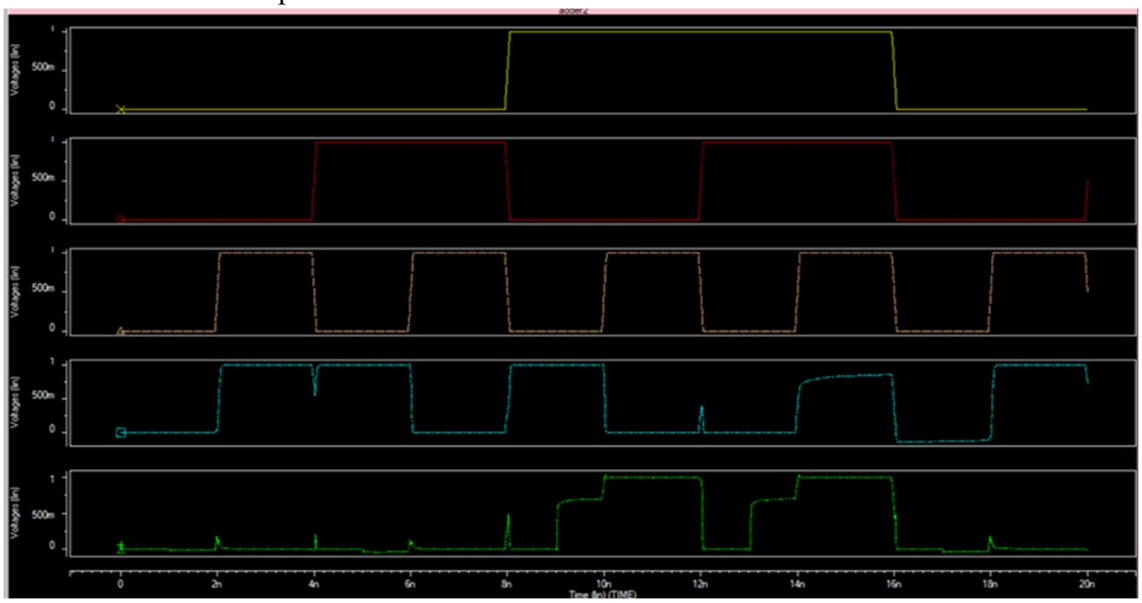
4. Results and simulations of proposed designs.

In this paper, all the design structures based on conventional CMOS logic and adiabatic logic are designed and simulated on cadence virtuoso using 90nm technology. The comparison is performed using different frequencies and supply voltages.

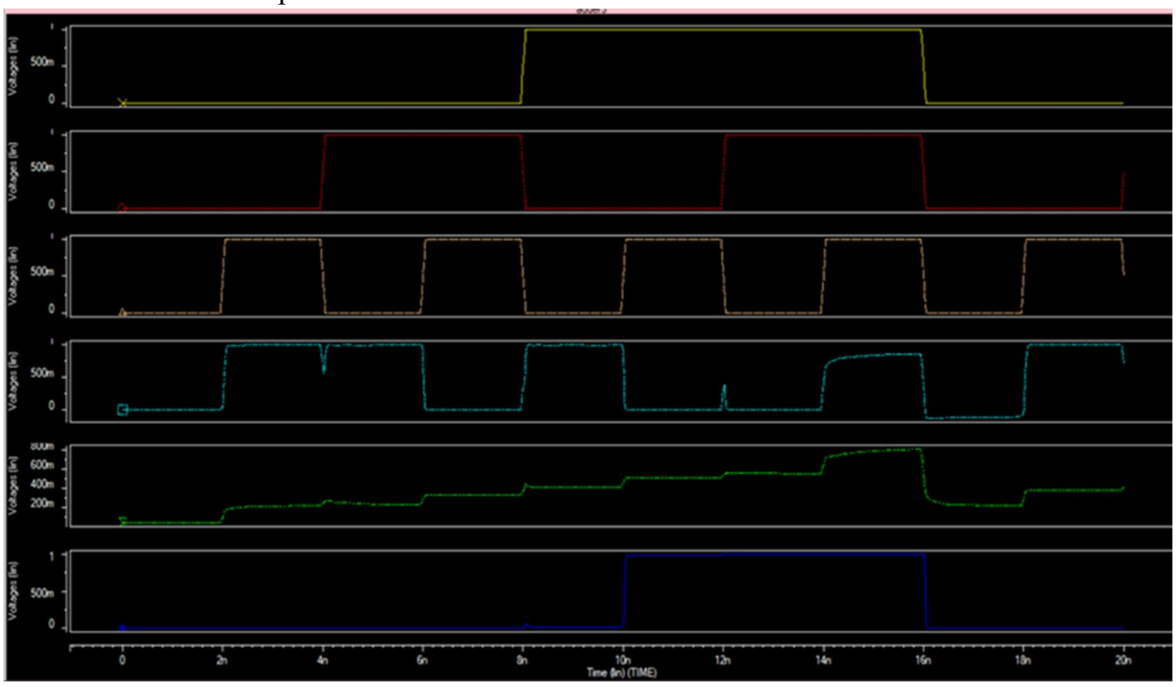
4.1 : Simulation of Proposed OF FULL ADDER-1



4.2 : Simulation of Proposed OF FULL ADDER-2



4.3 : Simulation of Proposed OF FULL ADDER-3



5. Conclusion

	No of Transistors	power	Delay
Adder-1	21(Nmos-10,Pmos-11)	2.618e-05	2.5e-012
Adder-2	23(Nmos-11,Pmos-12)	8.190e-05	3.23e-011
Adder-3	27(Nmos-13,Pmos-14)	1.517e-05	1.61e-010

In this article, implementation of parallel computing with adiabatic logic has been demonstrated for full adder designs. The work done in this article has been simulated in 0.18 µm CMOS technology. The proposed approach mitigates the issue of large propagation delay and achieves a signal restoration with a buffer. The presented designs perform better in terms of power dissipation, delay, and the number of transistors used as compared with the existing

designs which are reported in the literature. It is evident from the results that the overall power efficiency of the proposed designs is good as compared to existing designs. Implemented new circuits work fairly with varying voltage and temperature conditions. The proposed designs with adiabatic logic also perform better with sufficient output voltage levels. These improvements in performance with high speed make proposed full adders better candidates for ultra-low-power applications. As a future work, author is working actively toward the implementation of this approach in sequential circuits

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