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# DESIGN AND IMPLEMENTATION OFONE-BITALU USING REVERSIBLE LOGIC

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**ABSTRACT:** This paper presents a novel design of reversible logic based Arithmetic Logic Unit (ALU) which is efficient in comparison to the irreversible design in terms of power and area. In reversible logic design each input is mapped to a particular output therefore each output is known which prevent bit loss and reduces the power dissipation. The design ALU is simulated using Xilinx 2019.1 for logical verification. Further the design is synthesized and power comparison is done for both the reversible and irreversible ALU. It is observed that dynamic logic power is reduced by 53% and area by 20%.

**KEYWORDS—**Reversible logic, garbage output, dynamic power.

## Introduction:

For the applicability of the Moore's Law in the upcoming decades need new design technologies which necessitates to address the power dissipation problems in the CMOS based integrated circuits. Reversible logic synthesis is one of the promising technologies which address the power dissipation issue and theoretically claim that dynamic dissipation power can be reduced to 100 percent. Landauer in 1960 published in the IBM journal that using irreversible gates KT ln 2 energy is dissipated for one bit loss [1]. Later on, Bennett shows that if we use reversible logic gates with equal number of input and output where each output is produced by a known combination of the inputs therefore one bit loss can be avoided [2]. ALU is one the most important combinational logic circuits utilized for the arithmetic and logical computations in the computers. For extensive logic computation power dissipation in these types of circuits is a very dominating concern. Therefore, it is a focused area of research to reduce power dissipation in the ALU logic circuits. Reversible logic based ALU can solve this problem to a larger extent by significantly reducing dynamic power dissipation. In past few years a few articles have been published for reversible based ALU and the optimizing parameters are area and power. The limiting factor in the reversible design are ancilla inputs, garbage outputs and area [3-7]. Reversible logic based three variants of the adders is presented by P.K. Lala et.al.[8]. The designed reversible circuits are improved in terms of gate count and power dissipation. Binary reversible logic gates with quantum gates are proposed by Majid Mohammadi et.al.[9] A quantum cost efficient is presented by Rahman et. al. which proposed a two-qubit quantum gate library [10]. The current work reports one bit arithmetic and one bit

logic unit with special reference to the optimization of the area and power dissipated by using Xilinx 2019.1 and further verified by dumping the synthesized code in the FPGA kit. It shows the reduction in the dynamic power dissipation about 50% and 29% reduction in the area in comparison to its irreversible implementation.

**Proposed Structure:**

The propose 1-bit ALU consists of three units i.e., multiplexer, arithmetic and logic unit. The 2:1 multiplexer is used to integrate both arithmetic and logic unit together as shown in the figure 1. This ALU is designed to perform the function listed in the table 1. The block diagram of purposed Arithmetic Logic Unit designed through reversible logic gates is shown in composed of two unit viz. Arithmetic Unit and Logic Unit further output is given through 2:1 mux and output are given at fun. inputs are given to A and B and output is taken from fun of A 2:1 MUX is used for multiplexing Arithmetic unit and logic unit. Functions performed by this ALU are listed in the table I.

**Table I: Functional Table for 1-bit ALU**

| S | S0 | S1 | $C_{in}$ | Fun |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | A+B |
| 0 | 0 | 0 | 1 | A+B+1 |
| 0 | 0 | 1 | 0 | A+B’ |
| 0 | 0 | 1 | 1 | A-B |
| 0 | 1 | 0 | 0 | A |
| 0 | 1 | 0 | 1 | A+1 |
| 0 | 1 | 1 | 0 | A-1 |
| 0 | 1 | 1 | 1 | A |
| 1 | 0 | 0 | X | XOR |
| 1 | 0 | 1 | X | AND |
| 1 | 1 | 0 | X | OR |
| 1 | 1 | 1 | X | NOT |

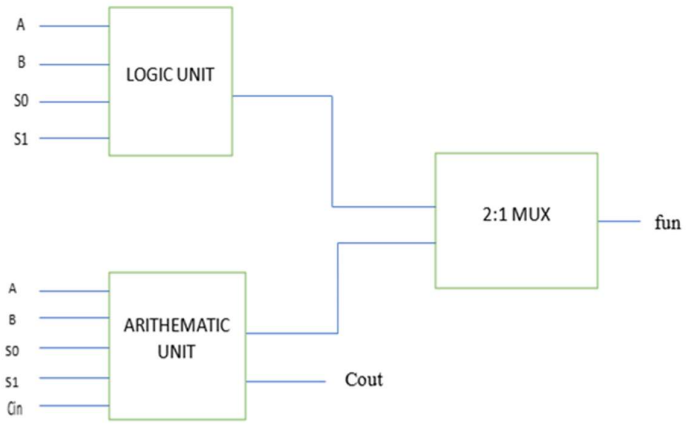


Figure 1: Block diagram of purposed ALU

## 2.1 Arithmetic Unit

1bit purposed structure of Arithmetic unit is as shown in figure 2 composed of 3 Toffoli gates, one Feynman gate and one DPG gate is used. DPG gate is used as full adder and Toffoli gate with Feynman gate provide the control mechanism which gives various arithmetic functions. The single arithmetic unit have four ancilla input and 5 garbage outputs. The Boolean equation for the Arithmetic is: For DPG gate we have three inputs i.e A, Y_1and Cin. Y_1, sum and C_out are given by equation (1), equation (2) and equation (3) respectively.

$$Y_1 = \bar{S}_0(S_1\bar{B} + \bar{S}_1 + B) + S_0S_1 \quad (1)$$

$$sum = A \oplus Y_1 \oplus C_{in} \quad (2)$$

$$C_{out} = AY_1 + Y_1C_{in} + C_{in}A \quad (3)$$

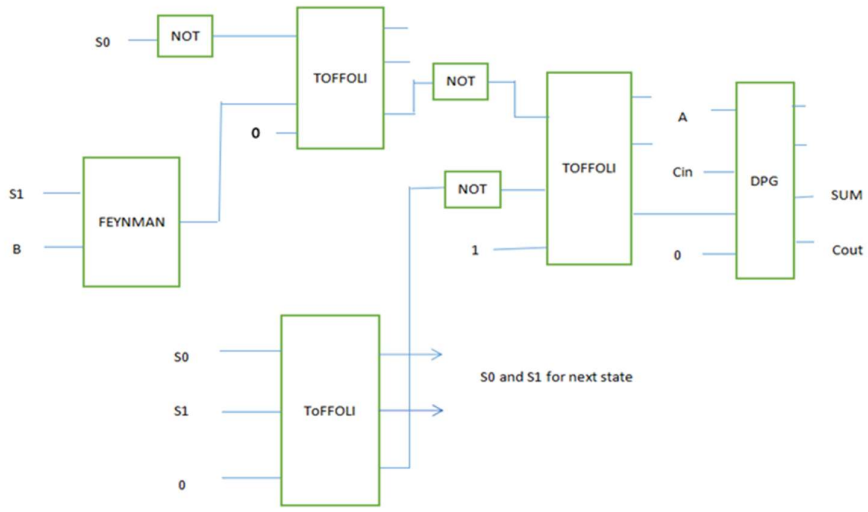


Figure 2: 1-Bit Arithmetic Unit

## 2.2 Logical Unit

1 bit logic unit is composed of two 4*4 Toffoli gate , one 3*3 and one 5*5 Toffoli gates and one Feynman gate is used for the logic structure this purposed as shown in figure 8 performs four basic logic

operations viz. AND , OR , XOR and NOT .Boolean equation for the logic unit is given by equation (4).

$$Y_1 = \bar{S}_1(A\bar{B} + B\bar{A}) + \bar{S}_0AB + \bar{S}_0S_1AB \quad (4)$$

This reversible logic unit has 4 ancilla inputs and 6 garbage output. It provides great reduction in the logic power in comparison to the irreversible logic unit.

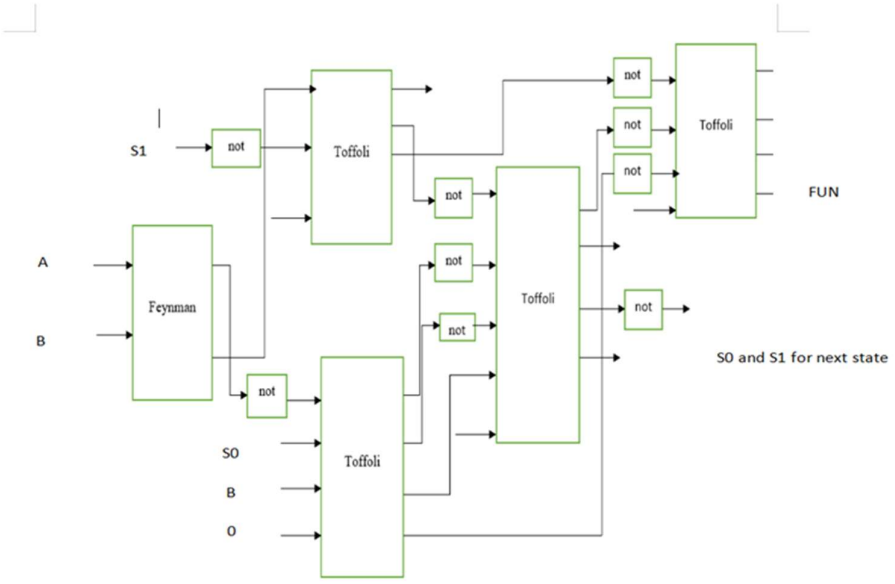


Figure 3: 1-Bit Logical Unit

### 2.3 2:1 MUX

2:1 MUX is used for combining the two unit viz arithmetic and logic unit together. Here mux is realized is using three Toffoli gates as shown in figure

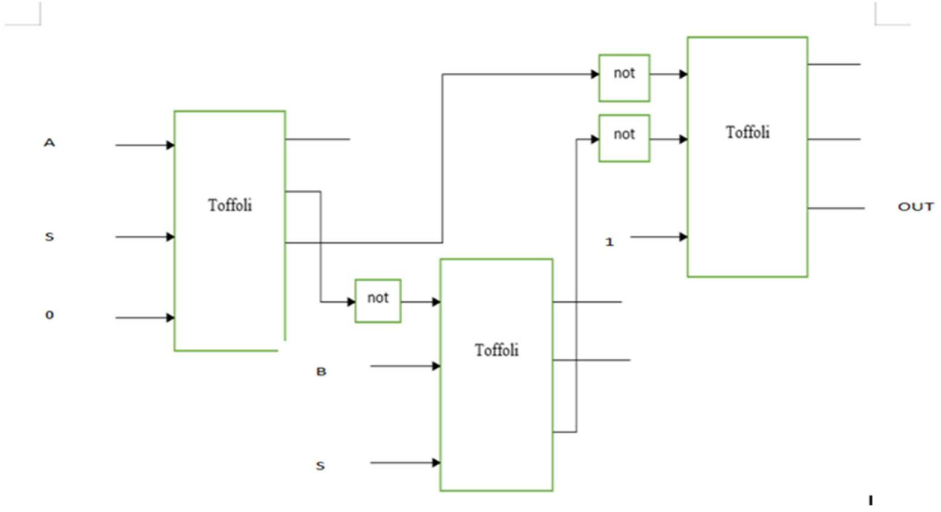


Figure 4: 2:1 mux

## 3.SIMULATION AND ANALYSIS

### 3.1 Simulation:

In order to check the correctness of the design simulation is performed by using Xilinx software. The Verilog language is used for the digital design entry. The structural level scheme of Verilog is used to facilitate synthesis smoothly. The arithmetic and logic units are simultaneously taken with the help of the 2:1 Mux. As per the select lines the function performed by the ALU are listed in the table I. The simulation was performed before as well as after the synthesis also. The RTL diagram is shown in the figure 5. The timing waveform is shown for the one-bit ALU design for different combination of inputs for arithmetic, logic &

MUX unit shown in the figure 6, figure 7 and figure 8 respectively. Figure 9 gives the synthesis report, the structural coding in is done in Verilog for making RTL code synthesizable.

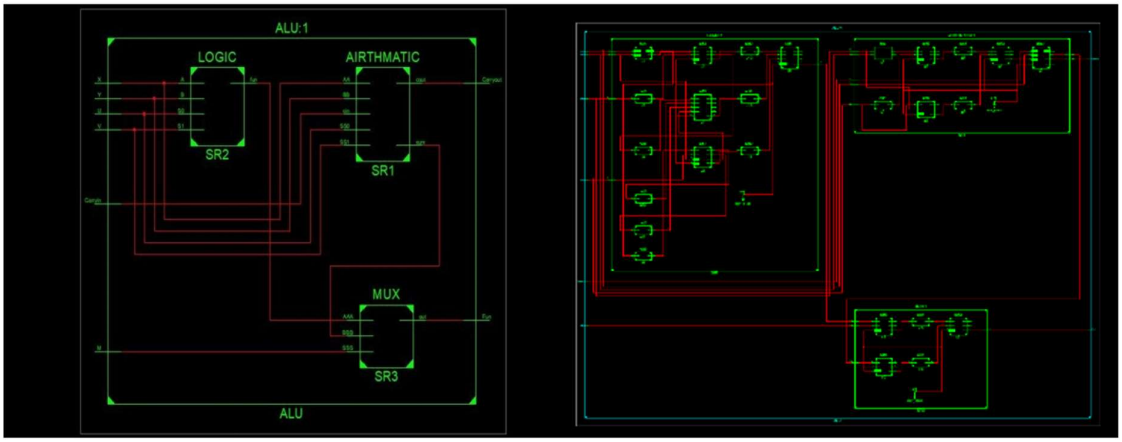


Figure 5: RTL Schematic of ALU

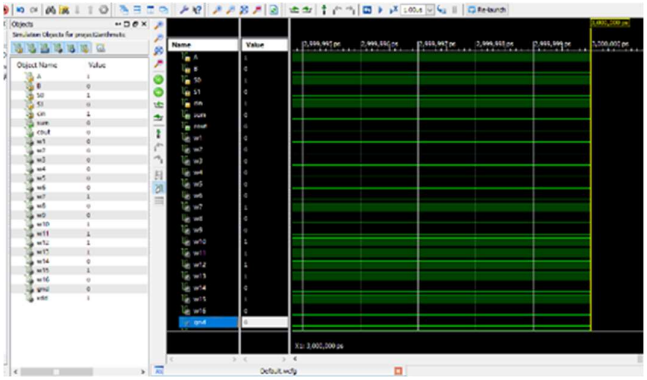

Figure 6: Simulation of the Arithmetic Unit

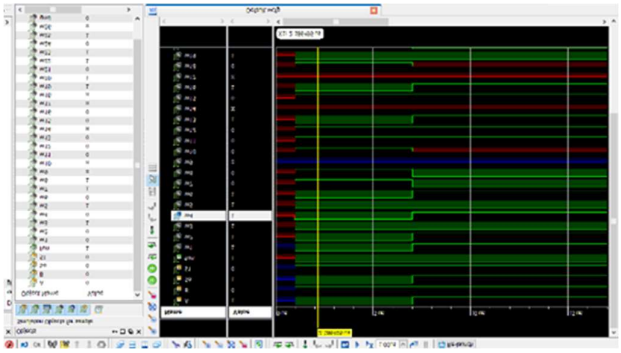

Figure 7: Simulation of Logic Unit

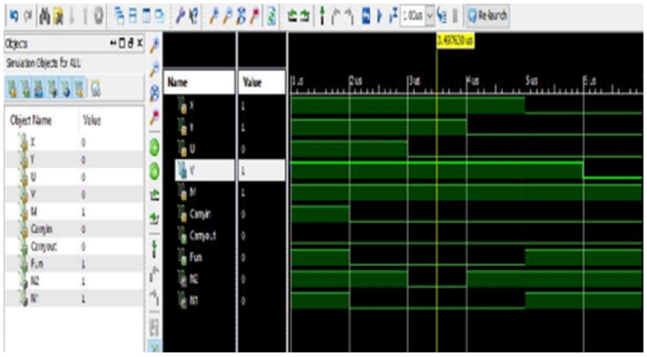

Figure: 8 Simulation of 2:1 MUX unit

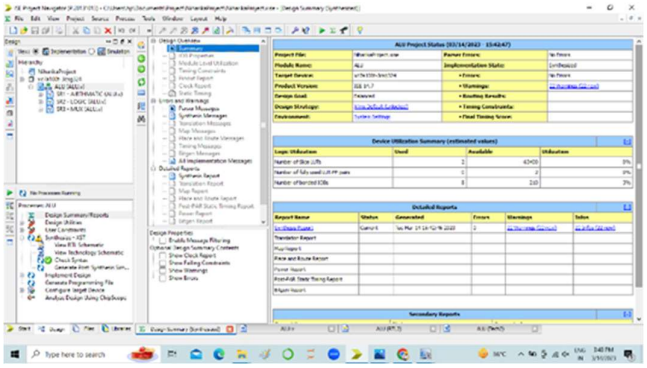

Figure 9: ALU Synthesis Report

### 3.2 Power Analysis:

Power analysis is one of the most important analyses in digital design, as any electronics engineer or researcher is in the process of optimization of the three main parameter which are area, speed and power. Area is to be minimized, speed to be enhanced and power dissipation should be small as possible. Therefore, reducing power dissipation is one the thrusting parameter in the design cycle. Before going in to the power analyses, one has to understand the importance of the signal rate or activity rate. This is the number of times a signal switches either from '0' to '1' or vice versa. Now the main components of the power dissipation are two types viz. static or standby power and dynamic or active power. The static power is the power consumption by the device when thedevice is not actively working i.e., from biasing of the circuits. The dynamic power is the power consumed by device after getting on i.e., when the device is actively clocked.This dynamic power further consists of input/output power, data power and logic power. The input/output power is the power dissipation when the device is power up but no logic is utilized and contributed due to various inputs and outputs. Data power is the power dissipation due to the switching activities happenings in the device. There is a reduction in this power dissipation when we are using reversible logic design in comparison to the irreversible logic design. The last one is the logic power; it is the power dissipation when some logic is realized in the device. It is the prime of focus of the reversible logic synthesis design, as theoretically it becomes zero for the reversible design device. In our design in comparison to the irreversible logic design the logic power has been reduced by more than 53% and at the same time area also has been reduced by around 20% in comparison of the irreversible logic design (Table II and Table III).

**Table II: Power analyzer report for 1-bit reversible ALU**

| Parameters | Arithmetic Unit | Lotic Unit | ALU |
|---|---|---|---|
| Slices | 2 | 1 | 2 |
| LUT's | 2 | 1 | 2 |
| I/O Buffer | 5 | 5 | 8 |
| Delay (ms) | 7.8 | 7.7 | 7.9 |

**Table III: Power dissipation comparison**

| Power Parameters | 1-bit irreversible ALU (mW) | 1-bit Reversible ALU (mW) |
|---|---|---|
| I/O | 2.17 | 2.17 |

| | | |
|---|---|---|
| Data | 0.14 | 0.08 |
| Logic | 0.15 | 0.07 |
| Total | 2.46 | 2.32 |

## CONCLUSION

A 1-bit ALU has been designed and implemented in this work by using Xilinx 2019 software package. The primary optimized parameter in this work are power dissipation and design area. Instead of irreversible logic gates, the ALU designed by using reversible logic gates showed great reduction in the dynamic logic power dissipation which is around 53% and overall power dissipation is reduced by more than 5%.

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