Journal of Data Acquisition and Processing
ISSN: 1004-9037
https://sjcjycl.cn/
DOI: 10.5281/zenodo.777369

VEDIC MATHEMATICS BASED SQUARING CIRCUIT USING 32NM TECHNOLOGY

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Abstract— Vedic mathematics is centered on sixteen aphorisms/ Formulae and thirteen sub-aphorisms/ Formulae that touch almost all different chapters of mathematics. Out of these sutras, Dwandwayoga has a duplex property used to find a square of a number. This paper proposes a 32 nm technology-based optimized squaring circuit using the Vedic sutra in physical layout. The consequences are matched through an orthodox multipliers circuitry in addition to a Vedas multipliers circuitry that was premeditated by means of the Urdhvatiryagbhyam formulae. These proposed architecture shows a 94.41% improvement in power consumption over the conventional multiplier and shows 76.34% more than the Vedic multiplier. It also shows a remarkable 66.03% improvement in energy deferral product equated towards the Vedas multipliers and a 96.13% improvement than a conventional multiplier.

Keywords— Vedic mathematics, Dwandwayoga, square circuit, Vedic multiplier

I. INTRODUCTION

Shree Swami B.K. Tirthaji (1884-1960) was Jagadguru Shankaracharya of Puri. He was a scholar in mathematics, English, and Sanskrit. Between 1911-1918 he rediscovered Vedic mathematics by writing 16 “Ganiti sutras” and 13 sub sutras [1]. These sutras and sub sutras are derived from Atharva Veda. Using these sutras one can solve different mathematical problems in a very short period of time without using pen and paper.

II. VEDIC MATHEMATIC

For calculating the result of squaring a number, we can utilize the multiplier circuitry. There are two methods to calculate the multiplication of two numbers. one is the conventional method and the other is a Vedic multiplier using the Urdhvatiryagbhyam sutra.

conventional squaring part – According to the traditional process for squaring numbers, a multiplication technique is used in which the same number is multiplicand and multiplier. In this method shifting and adding processes take place as shown below.[2]

Vedic multiplication using Urdhvatiryagbhyam sutra- In this method multiplication process takes place as shown in figure 1. we get answers in one line as observed in figure 1. As depicted in figure 3, the necessary hardware components for a 4-bit Veda multipliers are as follows

$$
\begin{array}{cccccccccc}
 & & & & & A_3 & A_2 & A_1 & A_0 & \\
 & & & & & A_3 & A_2 & A_1 & A_0 & \\
\hline
 & & & + & A_3 & A_0 & A_2 & A_0 & A_1 & A_0 & A_0 & A_0 \\
 & & & A_3 & A_1 & A_2 & A_1 & A_1 & A_1 & A_0 & A_1 & \\
 & & + & A_3 & A_2 & A_2 & A_2 & A_1 & A_2 & A_0 & A_2 & \\
 & + & A_3 & A_3 & A_2 & A_3 & A_1 & A_3 & A_0 & A_3 & & \\
\hline
S_7 & S_6 & S_5 & S_4 & S_3 & S_2 & S_1 & S_0 & & & & &
\end{array}
$$

4 BiSt Veda multipliers were premeditated by means of a 2-bits Veda multiplier and Ripples carry adder. [3] These structural design of the 2-bits Vedic multiplier is depicted in Fig. 2. This process can be used for squaring numbers just like a conventional squaring unit. But Vedic multiplier is speedy compared to the conventional multiplier [4]

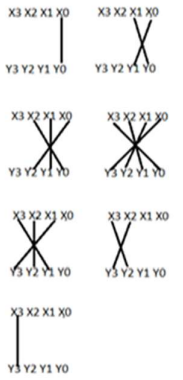

Fig. 1: 4-bits Veda multipliers algorithm using Urdhvatiryagbhyam sutra.

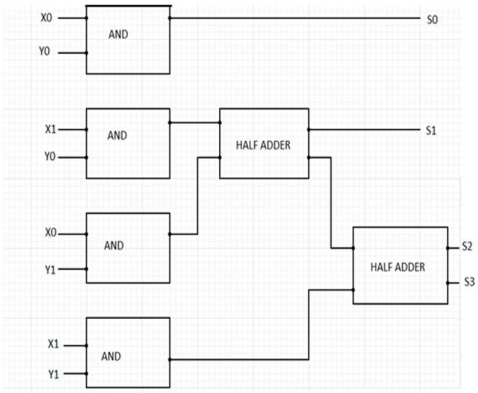

Fig.2: Hardware requirement of 2-bit Vedic Multiplier

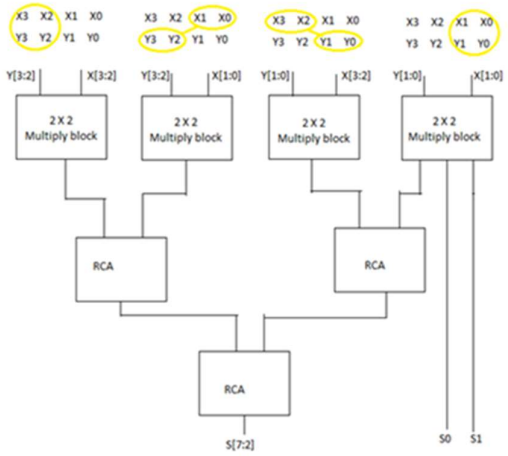

Fig .3: Hardware requirement using 4-bit Vedic Multiplier

This Vedic square algorithm is faster than Booths and Array multiplier. A conventional multiplier has more computations so more hardware is required and more time is consumed as compared to Vedic multiplier [5].

III. RELATED WORK

As area and power consumption are important parameters in VLSI technology, designers are working on new techniques to increase the speed and reduce the power consumption along with area reduction. Squaring circuit is an important part of digital ALU and DSP units. Conventionally multiplier circuit is used for squaring and cubing functions, it is advantageous to use dedicated units that require less power. The use of Veda sutras in digitalized filtering and analysis applications improves overall performance by processors [6]. The squaring function is used in finding division, reciprocal, and in finding roots also. [7,8,9] computation of square is also used in encryption and decryption process, [10]. The author [11] used squaring technique in finding power series. while in [12] authors showed the proposed squaring technique of the Taylor series using the Karatsuba-Ofman Algorithm. In this technique, the Duplex property is not used to reduce algorithm complexity. Using this technique inverse trigonometric series is also calculated with lower AMED. In [13] squaring and cubing unit is designed and synthesized using Artisan 90 nm. Here result shows that 40% area is occupied compared to the general multiplier. In [14] squaring circuit is implemented using various adder circuits using VHDL and synthesized through Xilinx ISE 14.2i. It is found that carry look-ahead adder is more efficient.

IV. PROPOSED SYSTEM

For calculating the square of four bits, the Vedic sutra "Dwandwayog" can be used. Dwandwayog had a "Duplex combination" which can be used for finding the the result of squaring a number. Following depicts a method for calculating the squaring of the N bits numeral.

E.g., D(P) = P2
D(PQ) = 2PQ
D(PQR) = 2PR + Q2
D(PQRS) = 2PS + 2QR
D(PQRST) = 2PT + 2QS + R2 and so on….

As shown in the above equation D can be calculated as the summation of the squaring of the intermediate numeral as well as twice the multiplication of other parts. The result of the squaring of the numeral is calculated as follows.

(PQ)2 = D(P) | D (PQ) |D (Q)
(PQR)2 = D(P) | D (PQ) |D (PQR) | D(QR) | D (R)
(PQRS) 2 = D (P) | D (PQ) | D (PQR) | D (PQRS) |
D (QRS) | D (RS) | D (R)

Illustration: For odd number
(25)2= (PQ)2= D (P) | D (PQ) | D (Q)
= 4 | 20 | 25
= 4 |2 0 |2 5
= 625

For Even number
(12)2= (PQ)2= D (P) | D (PQ) | D (Q)
= 1 | 4 | 4
= 144

V.EXPERIMENTS AND EVALUATION RESULTS

Here 4 Bit Vedic squaring circuit (Using Dwandwayog Vedic sutra) architecture using 32nm technology is implemented using the EDA tool with the BSIM4 model. Also, 4 Bit Vedic

multiplier circuit (Using Urdhwatiryagbhyam sutra) is also implemented and compared with the Vedic squaring circuit. Synthesis results are depicted in Tab 1. Fig 4 describes a layout of Vedic square circuit using 32nm technology whereas Fig 5 depicts the layout of 4-bit Veda multiplier using 32 nm technology. Their corresponding output waveforms are shown in Figures 6 and 7 respectively. Parameter comparison is as shown in figures 7,8 9. Results are compared for constraints such as Delays, energy, and Energy-Deferment lay Products for different architectures.

TABLE I. Analysis of Squaring circuits using a performance metric

	Area (μm^2)	***Delay (ps)***	***Power(µw)***
Vedic multiplier	649.5	37.4	65.64
Conventional multiplier	-------	49.8	433
Vedic squaring circuit	138.7	53.7	15.532

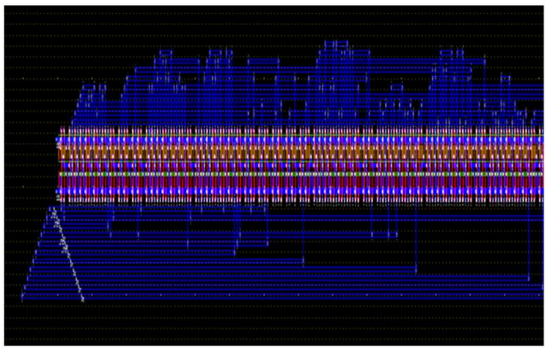

Fig 4.Vedic square circuit in 32 nm technology layout

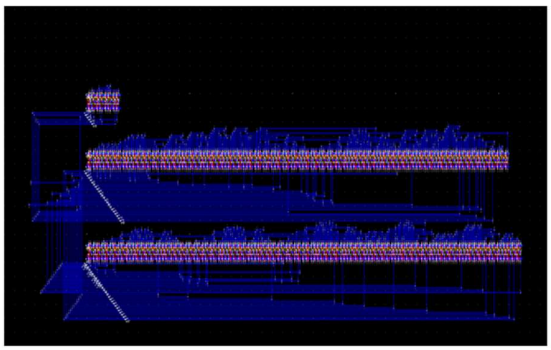

Fig.5:4-bitVedicmultiplier 32 nm technology layout

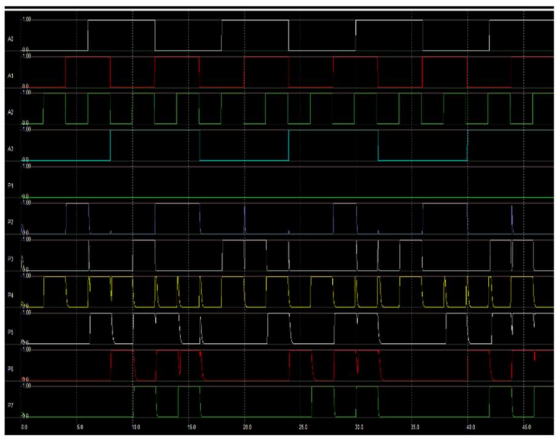

Fig. 6. Vedic square circuit waveform

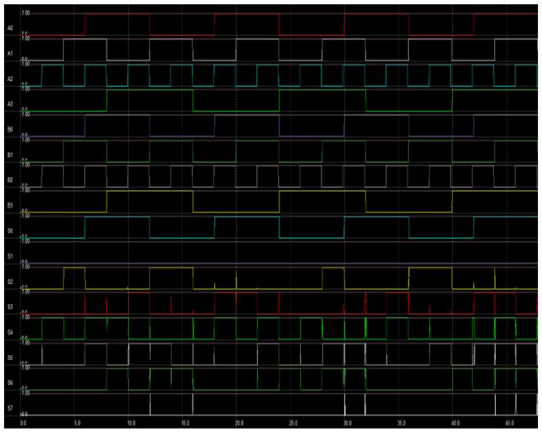

Fig.7. Vedic multiplier circuit waveform

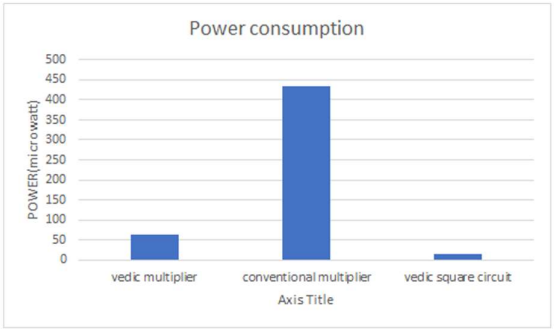

Fig.8 Performance comparison of Power consumption

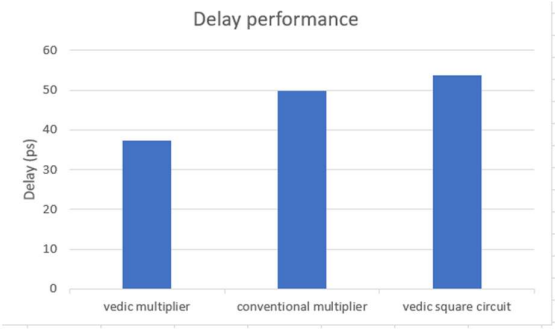

Fig 9. Performance comparison of Delay consumption

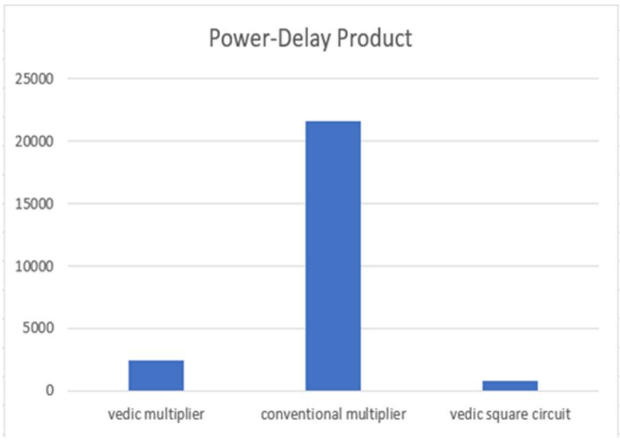

Fig. 10: Performance comparison of Power Delay Product

VI CONCLUSION

In this paper area efficient, low-power-consuming square circuitry is devised from Vedic mathematics. The analyzed result revealed that Vedic sutras not only reduced hardware requirement but also improves the effectiveness by means of delays, energy ingesting, as well as range than these conventional circuit. The proposed design shows a 94.41% improvement in power consumption over the conventional multiplier and a 76.34 % improvement over the Vedic multiplier. It also shows a 66.03% improvement in energy delays product equated to the Veda multipliers and a 96.13 % improvement than a conventional multiplier. Hence the Proposed architecture offers great improvement in area and power.

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