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QCA DESIGN OF FULL ADDER AND FULL SUBTRACTOR USING XOR GATE

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ABSTRACT:

In a recent times CMOS technology was replaced by the Quantum-dot cellular automata (QCA).It is because of Quantum-dot cellular is emerging designing technology in recent times. Circuits are fabricated by the quantum cells in QCA technology , its major advantage is its highly operating frequency and small size. Each unit in a QCA is called as cell and each cell consists of a four dots ,in that four dots two are electrons .Quantum dots are nanoscale structures which are constructed from semiconductors such as InAs and GaAs. The target is to implement the better design of full adder with mux logic and full subtractor with XOR logic for better performance . For that the fundamental blocks are majority gate, XOR gate .The existed methods contains 68 cells full adder with a clock cycle delay to over come that we came with a method so that cells are reduced to 21 cells and no clock cycle delays. where as for full subtractor we used a XOR logic to reduce number of cells to 20 cells. resulted decreasing the area occupation and clock delay.

Keywords: QCA technology, Majority gate, Multiplexer, Full adder, Full subtractor.

1. INTRODUCTION:

Designing a efficient circuit is the major task in any application. Previously we have used CMOS technology for circuit designing , but after a certain extent it is difficult to physically implement the circuit. As the nano technology is gaining popularity in circuit designing field and it is a one of the alternative to CMOS to implement the binary and multi valued logic circuits. QCA (Quantum Dot Cellular Automata) is the best one of the best tool to implement the low density , low power dissipations and switching frequency circuits. It has potential to revolutionize today's computing world and it is attracting more and more towards this field. QCA is a promising technology that has the potential to revolutionize the field of computing by enabling the development of faster and more efficient computing devices than what is currently possible with traditional silicon-based electronics.

At its core, QCA uses the charge configuration of quantum dots to transmit and process information. Quantum dots are tiny semiconductor particles that are capable of confining electrons in discrete energy levels. By arranging these quantum dots in specific configurations, researchers can create logic gates and other digital circuit components that can perform computations.

In this paper we initially learned about the majority gate and then we moved to 2x1MUX.Following that we designed the 4x1 MUX with the help of three 2x1 MUX by placing them concurrently. Using this concurrent arrangement and majority gate a full adder

was designed by using QCA. As all this was existed method ,we designed a full adder with QCA but with reduced cells and clock cycle delay. Which was reduced from 68 cells to 21 cells. And where as for full subtractor we used a XOR logic so that the number of cells was reduced to 20.

2. LITERATURE REVIEW:

Circuit designing is one of the major contributing factor in developing any application. By designing a proper circuit we can consume the power dissipation of system , its area occupied and also its performance. Numerous studies have been still going on to design a circuits with with great performance , low energy consumption and other factors. And there are many circuit designing technologies and one them is QCA.

Minimum feature in CMOS has reduced after several decades, however, facing some limitation. This subject caused the rapid development of molecular plans in Nano-scale. QCA is a hopeful sample in nanotechnology, suggested by Lent et al. and created in 1997.

1.“A majority-logic nano-device using a balanced pair of single-electron boxes,” published in Journal Of Nano-science & Nano-technology in 2002. Authors Oya, T., Asai, T., Fukui, T., Amemiya proposed a method to design single-electron integrated circuits. The gate device consists of two identical single-electron boxes combined to form a balanced pair. It produces a majority logic output by using imbalances caused by the input signals.

2 "An Efficient Design of QCA Full-Adder-Subtractor with Low Power Dissipation" published in Hindawi in 2021 by Ismail Gassoumi, Lamjed Touil, Abdellatif Mtibaa. In this the authors proposed about the 3 input XOR gate using QCA such that it reduces circuit size and also give low power dissipation.

3.“ Carbon nanotube field effect transistor (cntfet) and resistive random access memory (rram) based ternary combinational logic circuits,” published in Electronics in 2021. Authors Zahoor, F.; Hussin, F.A.; Khanday, F.A.; Ahmad, M.R.; Mohd Nawi, I.; Ooi, C.Y.; Rokhani, F.Z proposed that ternary designs (half adder, half subtractor, full adder, and full subtractor) have been implemented and simulated while using HSPICE and the results obtained from the simulation confirm the proper functionality of the proposed designs. When compared to the existing designs, the proposed ternary designs are superior in terms of the transistor count, power consumption, and reduced area.

3. METHODOLOGY:

3.1. Majority Gate:

In Majority gate performs a major functions on the inputs in Quantum-dot Cellular Automata (QCA). It take various input signals and produces the output signal which is the majority of the input signals.

In QCA the majority gate is made up of three quantum dots arranged in a triangular configuration. There are two states in each quantum dot: occupied and unoccupied. The output of the majority gate is determined by the state of the majority of the quantum dots. If the majority of the quantum dots are occupied then the output of the majority gate would be logical 1. And if majority of the quantum dots are unoccupied then the output of the majority gate would be logical 2.

For building various functions like AND, OR and NOT in QCA majority gate can be used. QCA is also used in designing QCA-based memory devices like shift registers and RAMs. Because of its simple structure and high speed operation, it is a future scope for nano electronic applications. MV3 means three input majority gate.

MV3= AB + BC + AC

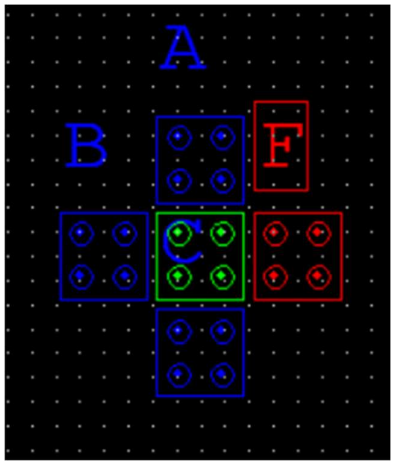

FIG 3.1.1: Majority Gate

3.2. XOR Gate:

A 3-input XOR gate is a logic gate that produces a output of logical 1 when any one of the three inputs is logical high (1) and all the three inputs are logical high(1). This is the functioning of the 3-input XOR gate.

In implementation of 3-input XOR gate in QCA, All the three input wires are crossed over each other with a series of majority gates arranged around the crossing point. And at this point majority gate compares the majority input from all the corners and gives output.

The 3-input XOR gate implementation is more complex then 2-input XOR gate in QCA designing. The 3-input XOR gates are very much useful to build the full adders, full subtractors, multiplexers and demultiplexers.

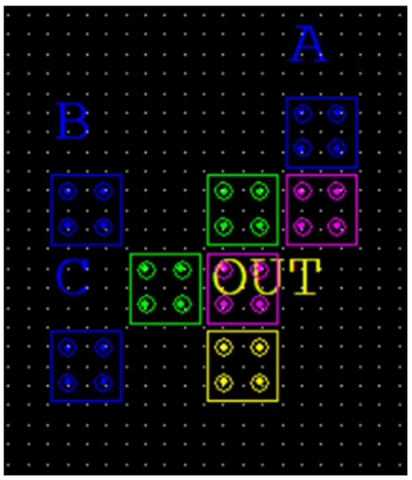

FIG 3.2.1: XOR Gate

4. BLOCK DIAGRAM:

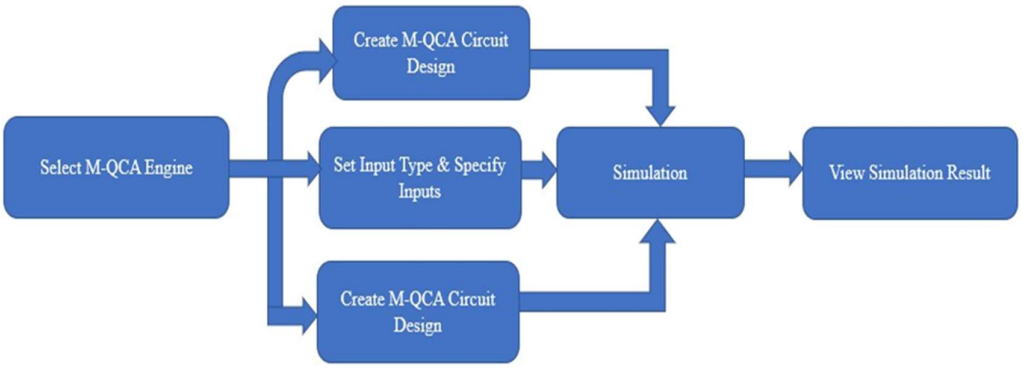

Fig 4.1: Block Diagram Of QCA Technology Implementation

Open the QCA designer tool and start creating the circuit by selecting cell icon on the left hand side. After selecting the cell we need to place it on the working area and according to the design select the clock cycles. Repeat this process to finish the circuit , now label the input and output pins according to the circuit requirement. After completion of this start simulation and at finally view the results of the simulation.

5. SUMILATION AND RESULTS:

5.1. Full Adder using MUX:

Here the full adder was designed using two 2x1 MUXs. We can see that the area occupied by it is 0.07 um^2 and consists of 68 cells. And of the major drawback was a clock cycle delay.

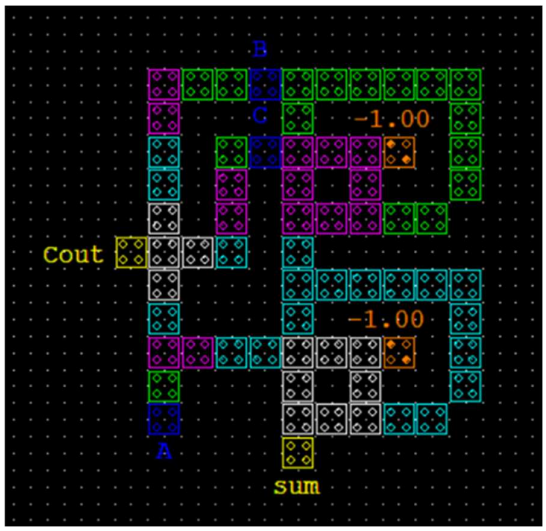

FIG 5.1.1: Full Adder using MUX

Now we can see the evaluation values which consists of area occupied by the circuit and number cells in a circuit.

File opened in 0.22 seconds
Selection extents: (146.00,68.00)[263.00x282.06] = 74181.35 nm^2 = 0.07 um^2 Objects selected: 68

FIG 5.1.2: Evaluation Table

Now we need to verify the end results to check its logic, whether its working properly or not.

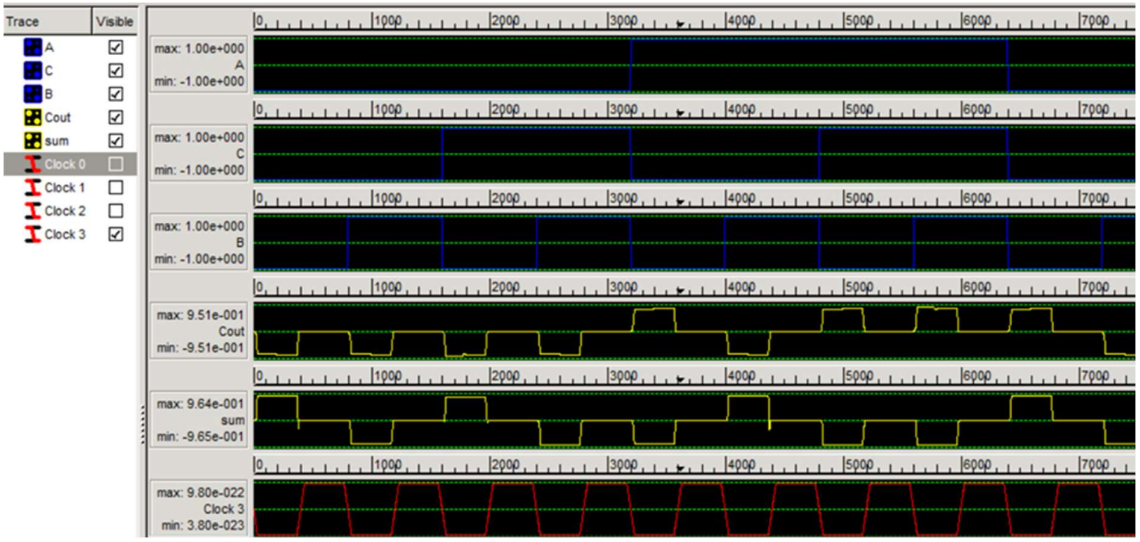

FIG 5.1.3: Result of Full adder using MUX with a delay in clock cycle

5.2. Full Adder using XOR with reduced cells:

Here we can see that the size of the full adder was reduced to 21 cells from 68 cells and also the delay in the clock cycle is also corrected.

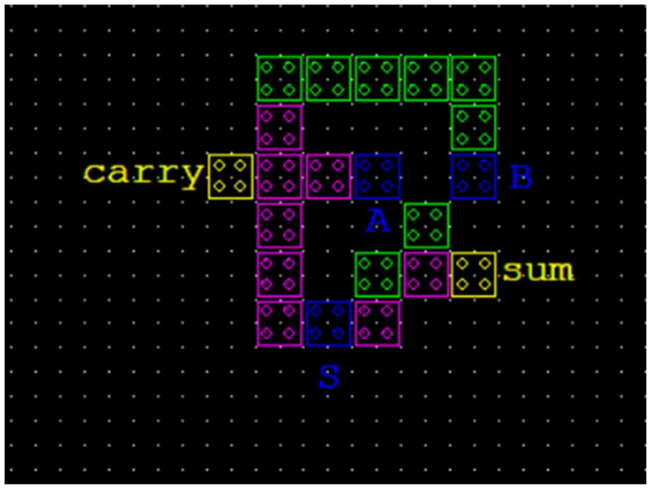

FIG 5.2.1: Full adder using XOR logic

Now we can see the evaluation values which consists of area occupied by the circuit and number cells in a circuit.

File opened in 0.12 seconds
Selection extents: (298.00,131.00)[204.24x141.87] = 28976.58 nm^2 = 0.03 um^2 Objects selected: 21

FIG 5.2.2: Evaluation Table

Now we need to verify the end results to check its logic, whether its working properly or not.

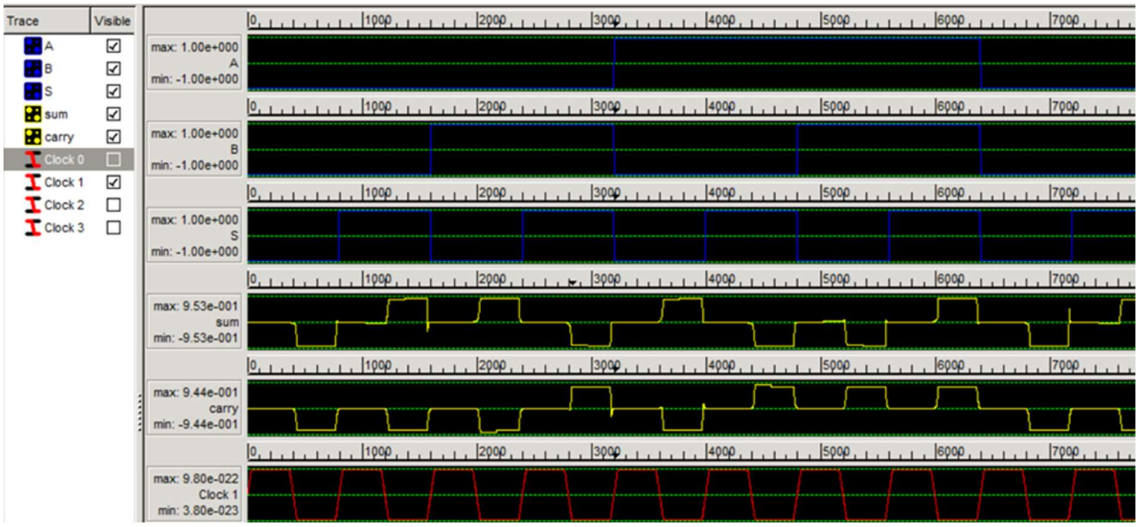

FIG 5.2.3: Result of the Full adder using XOR logic with no delay

5.3. Full subtractor using XOR logic:

Similar to the full adder with XOR logic this full subtractor with XOR logic also reduces its cells to 20.

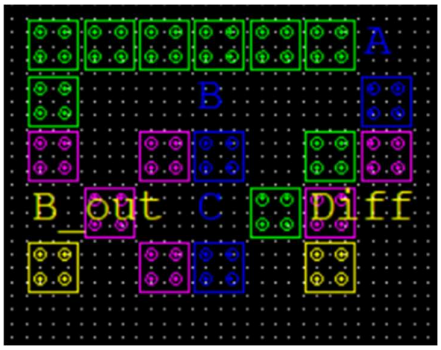

FIG 5.3.1: Full Subtractor using XOR logic

Now we can see the evaluation values which consists of area occupied by the circuit and number cells in a circuit.

File opened in 0.23 seconds
Selection extents: (291.00,108.00)[140.78x101.00] = 14219.21 nm^2 = 0.01 um^2 Objects selected: 20

FIG 5.3.2: Evaluation Table

Now we need to verify the end results to check its logic, whether its working properly or not.

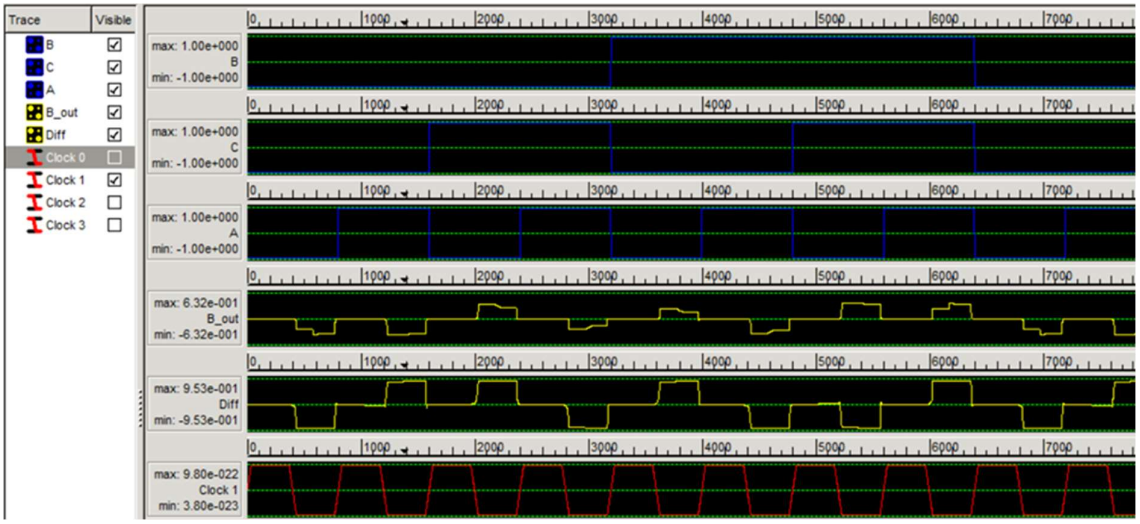

FIG 5.3.3: Result of the Full Subtractor using XOR logic

CONCLUSION:

In this paper we proposed a methodology so that one can switch designing from CMOS logic to QCA technology. As in the previous methods it was considered that implementing full adder and full subtractor with MUX, but designed them with the XOR logic. This XOR logic implementation provides us to reduce the circuit size by reducing the number of cells in it and also reduces its area, thus it improves the performance of the system. In full adder the cells are reduced to 21 and area was reduced to 0.03 um^2 and where as for full subtractor the are reduced to 20 and area was reduced to 0.01 um^2.

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