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MITIGATION OF SHORT CHANNEL EFFECTS IN FIELD EFFECT TRANSISTOR (FET) USING ALE WITH THERMAL APPROACH

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Abstract:
In this study, the problems of Gate All Around Field Effect Transistor (GAAFET) mainly its degradation parameters like short-channel metrics and leakage current in channels are discussed. It may be minimized by making some changes in fabrication of GAAFET on Silicon based semiconductor. SCE is a phenomenon that occurs in FETs with small gate lengths, where the gate controls the flow of current in a very narrow channel. At this scale, quantum mechanical effects become important, and the channel resistance increases, causing the drain current to decrease. This can be problematic for high-speed circuits, where a large current is required. One way to mitigate this effect is to use etching to create a recessed channel, which can help reduce the channel resistance and improve device performance. Etching can potentially decrease short channel issue in a FET, but its effect on leakage current depends on the specific etching method used and the properties of the FET itself. The changes are focused in etching on atomic layer of material based on Thermal characteristics such as earth-metals, metal-based oxides, semiconductor and their oxide-metals. The framework of this study is to expose basic principles on changes in the thermodynamic parameters of base-metal and corresponding response on their thermal metrics of earth-metal during etching procedure. In this type of etching process, a layer of minimum (Nano- meter) width layer of earth-metal is removed from base-metal using Atomic sized approach. This will be completed on self-timed sequential way for having a Self-control and self-saturation on the processed earth-metals. Various methodology of etching of earth-metals is reviewed and corresponding pros and cons is evaluated.

1. Introduction:

In the modern era, development on semiconductor makes a chip to be manufactured to be in nanometer scaled chipset. But smaller in size of chips will makes passive components fabricated on a chipset to be in smaller size [1]. Hence it is essential to move to Nano-sized passive components for development of semiconductor-based chip set board. For all type of chipset transistor will be unavoidable component for performing vital role in working of the chipsets.

But power dissipation in small sized transistor creates main headache for semiconductor manufacturing firms. The solutions for the above stated issues are given by GAAFET. It is an innovative technology that holds immense potential for the field of Nano electronics. It's a type

of transistor that has recently gained attention in the semiconductor industry. It is considered to be a potential successor to the currently dominant FinFET technology, as it has the potential to offer higher performance, lower power consumption, and better scalability. An outlined representation is shown in Figure 1(a)

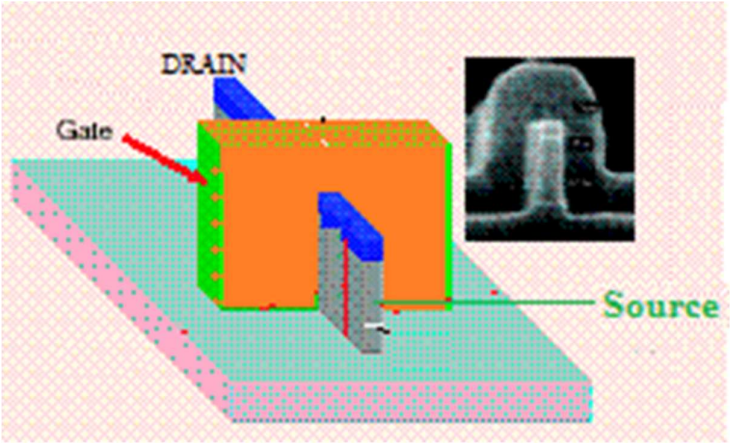

Figure 1 (a). Representation of a GAAFET [2]

There are several different variations in GAAFETs, including its vertical and horizontal type. The choice of structure depends on the specific application and design requirements [2]. Overall, GAAFETs represent an exciting development in the field of semiconductor technology, and they have the potential to drive innovation in a wide range of industries, including computing, telecommunications, and consumer electronics. However, more research and development is needed before GAAFETs can be commercialized and widely adopted. The basic structure of a GAAFET transistor consists of a nanowire that is surrounded by a gate on all sides, hence the name "Gate-All-Around".

The structure of GAAFET comprises a channel made of nanowire or Nano ribbon, which is surrounded by a gate material on all sides, enabling superior electrostatic control of the channel [3]. Here are some novel materials that can be used to design GAAFET structures:

1. Two-dimensional materials: GAAFET structures can be fabricated using two-dimensional materials such as graphene, Transition Metal Dichalcogenides (TMDs), and black phosphorus. These materials have unique electrical and mechanical properties that can enhance the performance of GAAFETs.
2. Nanowires: Nanowires made of materials such as silicon, germanium, and III-V compounds can be used as channels in GAAFET structures. These nanowires have a high aspect ratio and can be easily integrated with gate materials.
3. High-k dielectrics: High-k dielectrics such as hafnium oxide and zirconium oxide can be used as gate materials in GAAFET structures. These materials have a high dielectric constant, which enables better electrostatic control of the channel.

4. Ferroelectric materials: GAAFET architectures can utilize ferroelectric gate materials such as Lead Zirconate Titanate (PZT) and Barium Titanate (BaTiO3). These materials have a switchable polarization that can be used to modulate the electrical properties of the channel.
5. Organic materials: Organic materials such as Pentacene and Tetracene can be used as channel materials in GAAFET structures. These materials have high charge carrier mobility and can be easily processed using solution-based techniques.
6. Topological insulators: Topological insulators such as Bismuth Telluride and Bismuth Selenide can be used as channel materials in GAAFET structures. These materials have a unique electronic structure that enables the transport of charge carriers with spin- momentum locking.

Overall, the selection of materials for GAAFET structures depends on several factors, such as performance requirements, fabrication processes, and compatibility with existing technologies. Further research is needed to optimize the performance of GAAFET structures using novel materials. This design allows for better control over the flow of electrons through the transistor, as the gate can completely surround the channel region. In addition, the nanowire structure allows for better electrostatic control, which can improve performance and reduce power consumption. But

the problem is not solved fully because GAAFET type of components has two major metrics for their performance degradation 1) Short channel effect 2) current leakage in layers.

1.1 Factors used on decreasing short channel influence and current leakage on GAAFET: As the size of transistors falls below 10nm, short channel effects (SCE) have emerged as a significant impediment to transistor technology [4]. These effects can result in deviations in transistor properties, leading to reduced performance and device malfunction. A possible solution to counteracting SCE is to employ Atomic scaled Layer Etching (ALE) in a thermal line of attack. It refers to a method that utilizes a sequence of self-limiting chemical reactions to accurately remove thin layers of material atom by atom. The technique can be leveraged to selectively etch materials from the sidewalls of a transistor channel, which can help to mitigate SCE by reducing the effective channel length. The thermal approach involves employing heat energy to enhance the etching process. This method can expedite the etching process and render it more manageable to regulate.

1.2 Benefits of Atomic scaled type of etching in decreasing current leakage and short channel metrics:

The type etching can aid in decreasing the leakage current of GAAFETs by reducing the effective channel length and thus mitigating the impact of short channel effects (SCEs). By selectively etching the material from the sidewalls of the transistor channel, ALE can create a well-defined, uniform channel structure with a high aspect ratio. This enhances electrostatic control over the channel and reduces the probability of current leakage. Additionally, ALE-type etching has the capability of achieving precise control over the channel geometry, allowing for the fabrication of sub-10nm devices with minimal variation in device characteristics. This ultimately results in improved device performance and reduced power

consumption. Overall, ALE-type etching is a promising technique for reducing leakage current and improving the overall performance of GAAFET structures.There are several potential benefits of utilizing ALE in thermal approach for mitigating issues in less than 10nm:

1) Improved precision: ALE in thermal approach enables highly precise etching of materials with atomic precision, which can help to reduce the effective channel length of the transistor, thereby mitigating the SCEs.

2) Reduced process variation: The thermal approach in ALE can reduce the process variation and improve process control, resulting in more uniform device characteristics.

3) Faster process: The use of heat energy in the ALE process can expedite the etching process, reducing the time required to fabricate the transistor.

4) Increased device density: By reducing the channel length and mitigating SCE, ALE in thermal approach can enable the fabrication of high-density devices, which can increase the overall performance of the system.

5) Compatibility with existing technologies: ALE in thermal approach is compatible with existing semiconductor manufacturing processes, enabling its integration into current fabrication technologies.

6) Enhanced control of Etch Process: ALE in thermal method can enable improved control of the etching process, leading in more precise material removal from the sidewalls of the transistor channel. This can help reduce the effective channel length and mitigate SCE.

7) Selective etching of materials: ALE can selectively etch certain materials, which can be useful for removing unwanted materials from the transistor channel without damaging other materials.

8) Atomic-scale precision: ALE has atomic-scale precision, which means that the etch process can be controlled with extreme precision. This can be particularly useful for reducing the effective channel length and mitigating SCE.

9) High etch rates: The use of thermal energy can enhance the ALE process, resulting in higher etch rates. This can help reduce the processing time and increase throughput

Overall, the use of atomic scaled etching treatment in thermal based offers several potential benefits for mitigating issues in less than 10nm transistors [5], resulting in improved device performance and reduced power consumption.

In spite of thermal treatment based etching procedure has more vital benefits than other variety of etching procedure followed in fabrication cycles. Some of the notable benefits are.

1) Improved selectivity: The thermal approach in etching of GAAFETs can provide better selectivity, which enables the precise removal of specific materials while leaving others intact. This allows for the creation of complex structures with high accuracy.

2) Enhanced control: The use of heat energy in the etching process allows for better process control and faster reaction rates, resulting in more uniform and precise features.

3) Reduced damage: The thermal approach in etching of GAAFETs can cause less damage to the surrounding materials, resulting in higher quality features and better device performance.

4) Compatibility with a wide range of materials: The thermal approach can be used to etch a variety of materials, including metals, oxides, and nitrides, making it a versatile technique for fabricating GAAFETs with a wide range of channel and gate materials.
5) High aspect ratio structures: The thermal approach can enable the fabrication of high aspect ratio structures, such as deep trenches and narrow channels, which are important for creating GAAFETs with improved performance.
6) No chemical wastes: Thermal etching, unlike wet and dry etching, does not produce chemical waste making it a more environmentally responsible solution.

The development on semiconductor industry makes an etching process of Atomic-sized procedure to be a most promising fabrication of different earth-metals. This process will vary in accordance to fundamental thermal characteristics of metals. Especially for handling etching of nano-sized earth metals. Various conventional etching methodology like Plasma- based, Florence- based etching technique to be Cost-effective than Atomic sized etching procedure. Also conventional type may create physical damage on the semiconductor due to their non-precision etching process. This makes a need of minimal sized etching procedure leads to Atomic scaled etching practices.

Initially Atomic-scaled etching procedure-based ions present in the earth-metals in a specific area on semiconductor. This category of etching termed as directional etching procedure as etching will be carried out in a specific guiding on semiconductor metals based on their ions present in the semiconductor. The directional of etching is a horizontal direction in metals using various ions- based films.

For heat treatment-based etching will be done in all direction in the etching location of a semiconductor. This type of etching does not in need of any guidance on the etching process because of their etching procedure carried equally in all direction of semiconductor's etching location. Hence it is an efficient etching methodology in a fabrication of semiconductor.

This is a crosswise- directional etching in an Atomic-sized way results in materialization of electric-channels in a semiconductor metal to be active in transverse direction on sidewall

of a supporting semiconductor structure [6-7]. It makes suitable for three-dimensional fabrication for defense-based fabrication procedure.

Because of its stable etching rate and accurate processing time on etching procedure to be used in most of health based and defense-based fabrication structure. In recent years, need of minimal sized fabrication materials needs an atomic scaled etching procedure of less than 5 nano-meters. Also, this type of etching will be carried out in a layer-to-layer fabrication steps on semiconductor. But conventional type of etching techniques will not meet these minimal sized etching processes.

For advanced applications [8-10], sometimes etching procedure will be done in a combination of deposit and thermal treatment based etching processes. This will result in an effective etching treatment even in a nanometer sized in fabrication steps. Hence it leads to ultra-fine etching route in an either in crossover direction or in traverse direction with ultra- smooth physical structure on a semiconductor.

2. Thermal based etching process and its contrivance

In a normal fabrication [11-13], thermal treatment-based etching carried by usage either neutralized gas or by a vaporized steam for making a smooth etching in nano-scaled location. As this is a sequential type of etching procedure, etching location and corresponding layer-to-layer width on semiconductor from the figure 1(b), Outer layer chemical-reacted absorption variant of thermal treatment will be based on etching procedure. The outer layer is initially absorbed using some chemical substances based on their etching location. In the figure1, it may depict that the etching procedure carried over in sequential manner with a predefined etching locations. This is for avoiding physical damages in semiconductor surfaces.

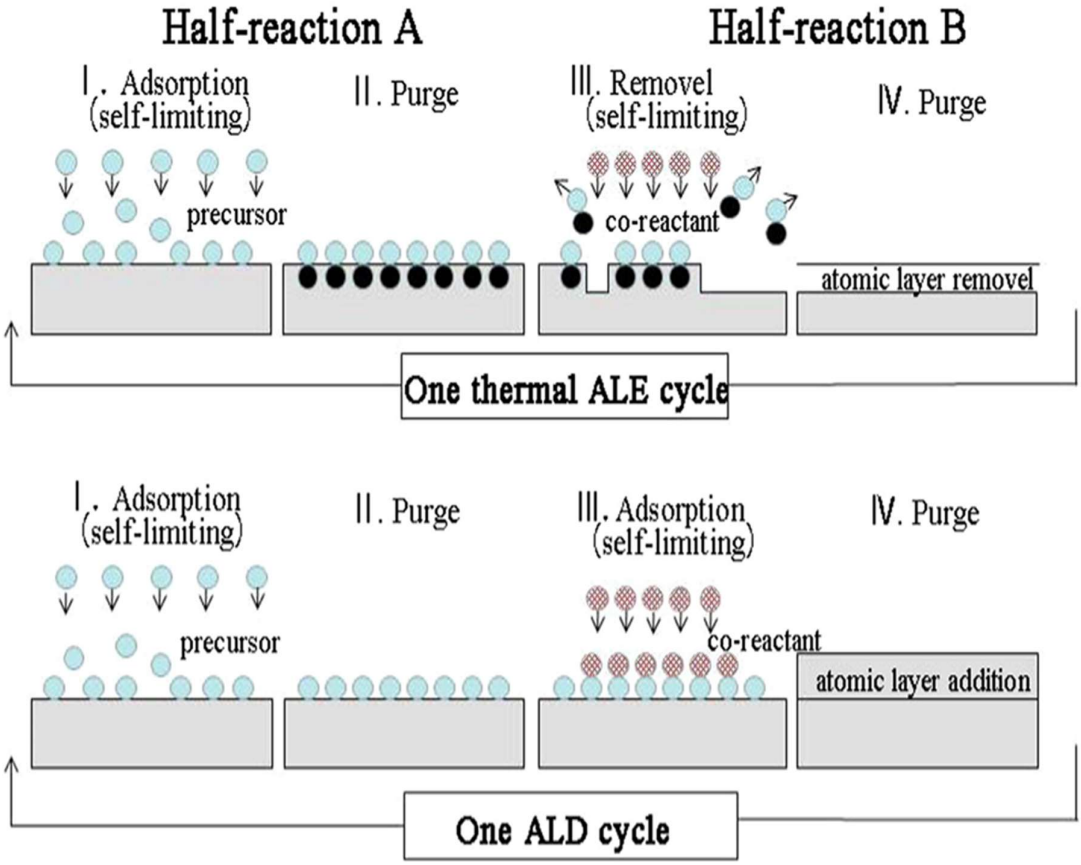

Figure 1(b). Illustration of thermal based etching procedure [15]

Depending on the fabrication growth rate, growth rate of layer should be defined for each and every step. Etching process rate should be defined before fabrication started. As thermal treatment based etching procedure is a sequential methodology self-controlled module in all etching steps.

As the initial outer layer removal is based on chemical composition, aluminum based chemical treatment is proposed for having a extreme small-sized etching with smooth curvature of etching location on the processed semiconductor. On comparing to other conventional chemical based layer removal [14-17], aluminum has maximum deductibility, adapting to thermal treatment. Hence, the proposed system has aluminum based thermal treatment etching and its performance is evaluated. In the proposed Aluminum flow mechanism is depicted in Figure 2(a) shows the flow of proposed methodology on introducing of Fluoride material and

evaporation of Water particles from semiconductor surface and Figure 2(b) represents chemical bonding of aluminum and fluoride chemical composition.

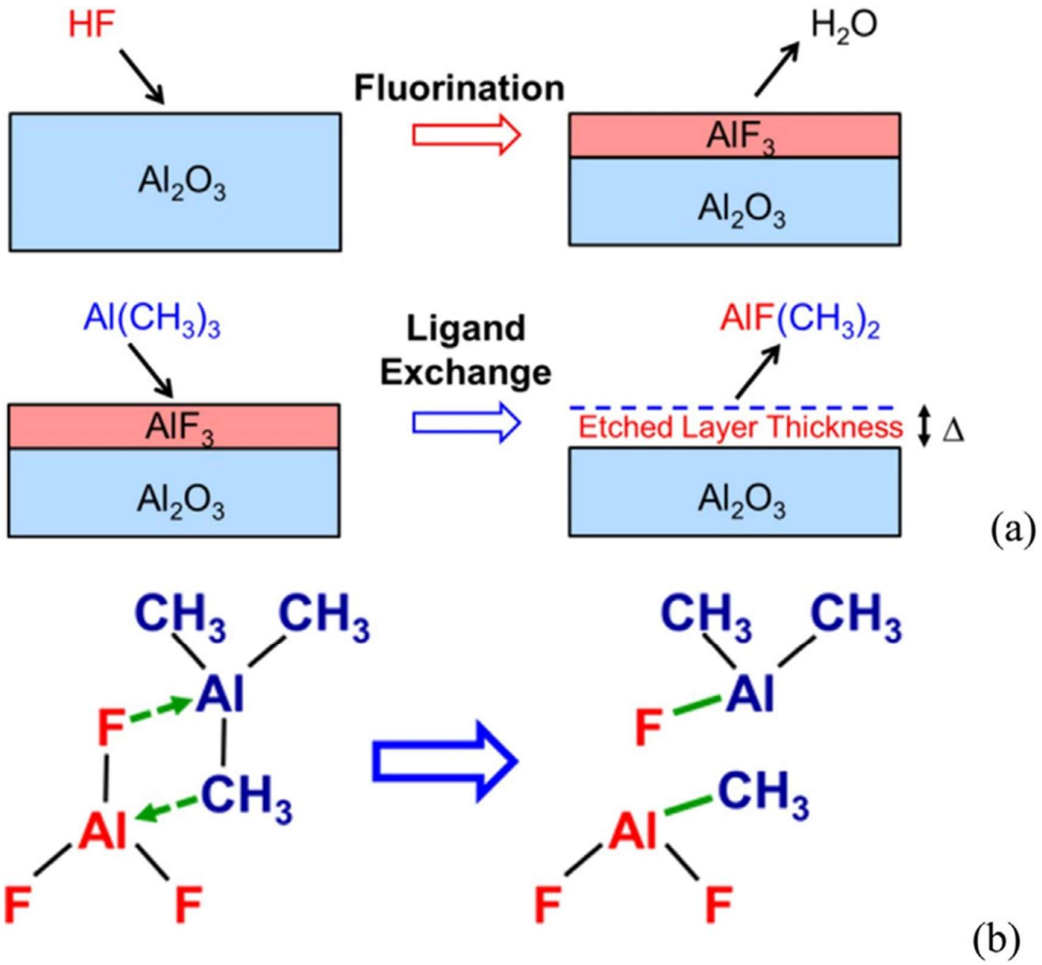

Figure 2 (a) & (b). Flow mechanism and Bonding structure of methodology [15]

3. Etching procedure using Aluminum based - Fluoride substances

As the combination of Aluminum and fluoride increases semiconductor adapting feasibility for etching procedure [18-20]. The chemical bonding of the chemical composition is given in equation (1)

$$Al_2O_3 + 6HF + 4Al(CH_3)_3 \rightarrow 6AlF(CH_3)_2 + 3H_2O \quad - (1)$$

The formation of chemical-based substances over the semiconductor is done in temperature of 150-260 `c. this temperature will be maintained throughout fabrication until outer surface is removed completely. After that etching location is defined for making a sequential etching treatment on the surface of semiconductor. By following the stable temperature and

chemical composition on semiconductor fabrication, surface will have roughness of 3-5 etching unit. Hence overall chemical bonding in the etching process is defined by equation (2).

$$Al_2O_3 + 6HF + 6Sn_2 \rightarrow 2Al_3 + 6SnF + 3H_2O \quad - (2)$$

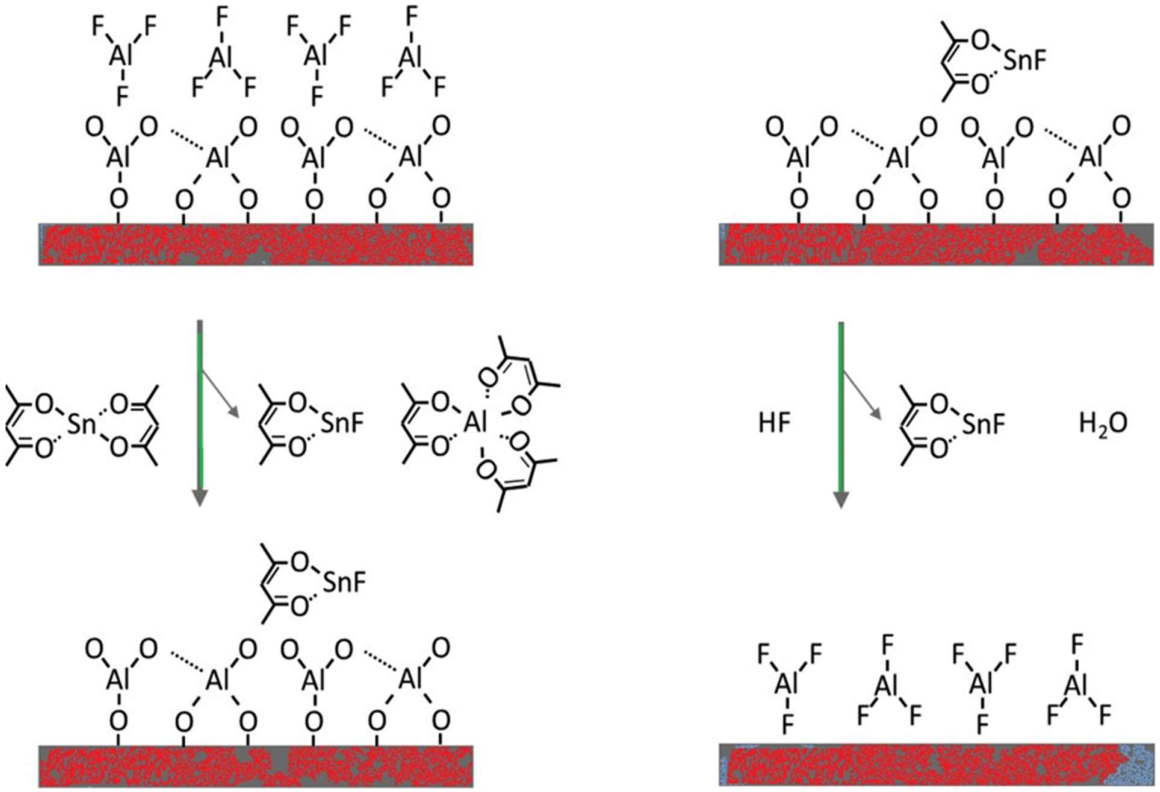

Figure 3. System's Diagrammatical Representation [19]

From the figure 3 we may understand the schematic representation of proposed system. The thermal treatment etching procedure will be a sensitive to temperature [21-24]. Hence, on the fabrication of chemical coated semiconductor right temperature is maintained throughout the removal of outer surface. Then with correct compositing of fluoride and aluminum etching is started on the supporting semiconductor surface.

On the etching is going on a semiconductor, we have to absorb the exposure time of a semiconductor to chemical used for etching process. This is because chemical may core substrate of semiconductor and results in unwanted surface damage. This will be measured in terms of number of cycles required for making a successful etching process on given area. From the figure

4, it will be proven that proposed etching procedure required minimum number of cycles even in high temperature (say 300 'c).

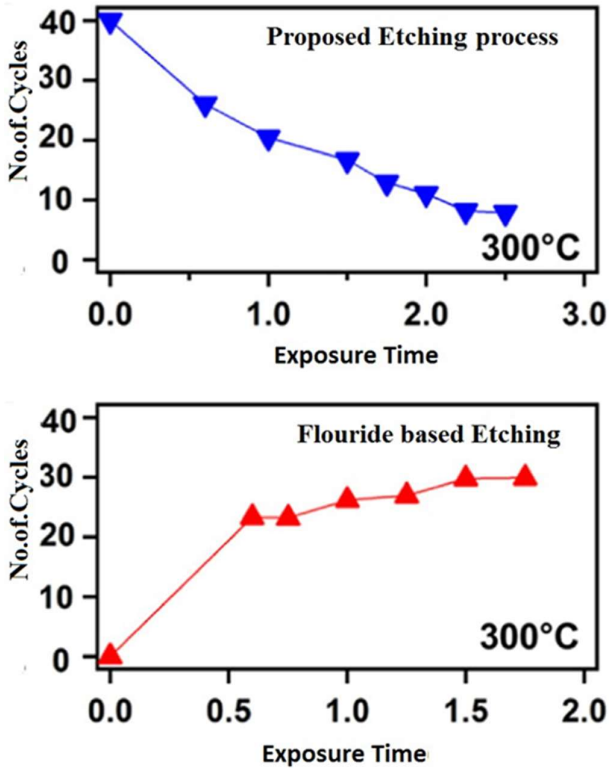

Figure 4. Exposure Time on Etching Process [19]

Also temperature on semiconductor should be decreased on finishing of etching process. If temperature becomes lower than initial stages of etching, semiconductor will able to move to other fabrication process. On other hand, if temperature goes on increasing due to any reaction happens after etching procedure get finished. This will makes damages both in outer layer of semiconductor and etched area of semiconductor. Hence it is important to minimize temperature of semiconductor after finishing of etching treatments on specific location of outer layer of semiconductor. From figure 5, it is shown temperature of proposed system based etching become lower than fluoride based etching treatments. Also it is described that proposed methodology etching has effectiveness in minimizing the outer surface temperature than fluoride based etching treatment processes. As etching is sequential fabrication process, lowering of temperature in outer surface of semiconductor is vital part of further fabrication process of semiconductor.

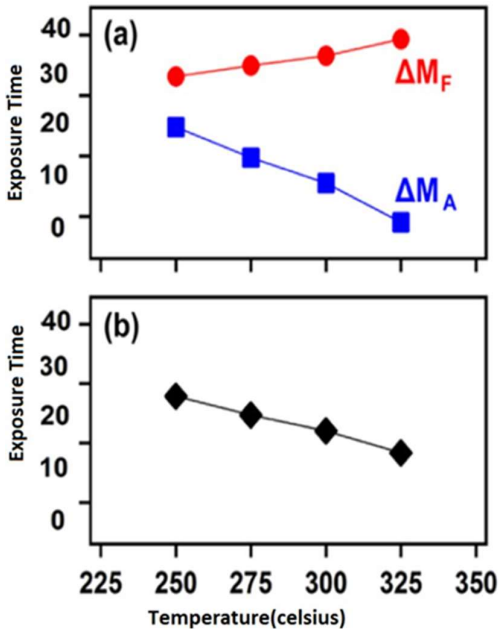

Figure 5. Dropping of Temperature on Outer Layer of Material [23]

Most of the etching treatment are temperature sensitive, because using heat only removing of unwanted materials from the outer layer will be done. It is a vital metrics as temperature increases chemical composition applied on outer surface of semiconductor. Hence we have to keep an eye on surface-temperature of materials. Also it is already shown that surface temperature of Aluminum based etching have lowered their surface temperature on comparison to surface temperature of fluoride based Etching.

It shows that proposed methodology have lowered their temperature on comparison to conventional fluoride based etching procedure. By making temperature lower in minimum span of time, other steps of fabrication is proceeded in fastest manner than conventional etching treatment. Hence, proposed Aluminum based etching makes fabrication process to be in ahead manner results in increases of manufacturing of Semiconductor based chips.

Next important parameter is to concentrate on the thickness of layers on completion of etching procedure. Normally in an etching process removal of unwanted materials from the outer layer of semiconductor is done by applying suitable chemical composition, as thickness of layers decreases on more number of cycles, it is said to be an efficient etching procedure. The impact of thickness of layer on etching process is discussed in the following representations.

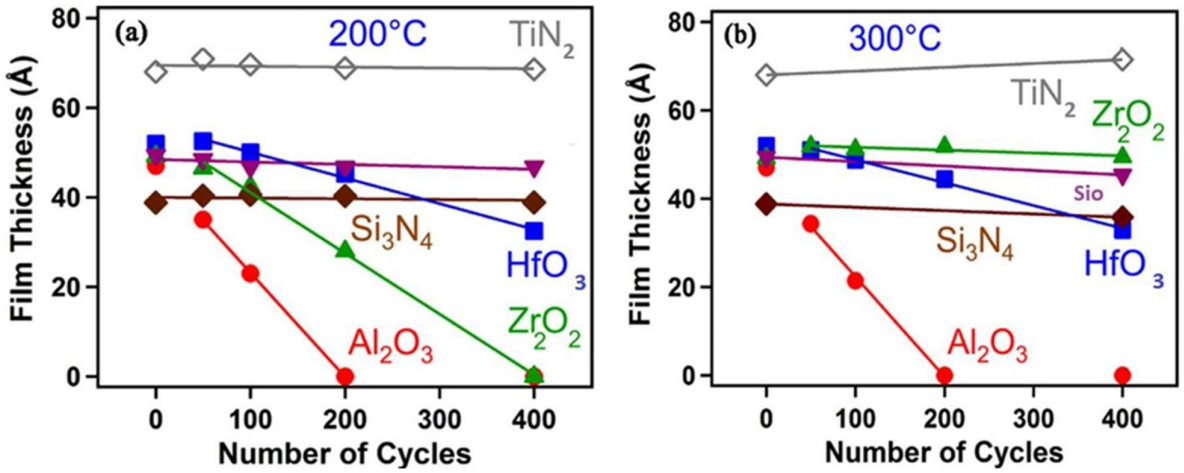

Figure 6(a)&(b). Comparison on Thickness of Layers [23]

On sighted on figure 6 (a), it is proven that this etching procedure have minimum thickness of layers on comparison to conventional etching procedure. This result is observed for various temperatures and results are shown in figure 6 (b). On increasing of surface temperature, proposed etching treatment requires minimum number of cycles. This shows efficiency of system even in high temperature maintained stable.

Table 1: Some distinctive ALE methodology and necessities.

ALE mechanism	**Reactants**	**Etched materials**	**Requirements**
Fluorination	HF_2/Sn_2	$Al(CH_3)_3$ $SiCl_3$	Steady non-volatile fluorides based chemical composition
Conversion on fluorination processes	SiO_2, ZnO	TiO_2, BCl_4	Transformed toward a dissimilar physical materials Al_2O_3
Oxidation- changing-fluoride processes	TiN_2	SiO_2, ZnO	Unchanging and volatile metal based-fluoride substances

The above table 1 describes different methodology followed in Thermal treatment based etching procedure and its reactants materials. From the table any chemical composition will suit with aluminum-based etching. But it should be made in correct chemical bonded substances.

The proposed system of etching procedure makes an etching treatment on a transversal direction. i.e., the removal of unwanted substances from the semiconductor should be done in an even way both in horizontal and vertical directions. By doing like this etching process will be in a self- controlled and self-limited in prescribed area on the semiconductor. The removal of unwanted substances from the outer layer is done in ultra-smooth manner which is graphically represented

in a figure 7. It is clearly shown that the etching tip moves in even both in horizontal and vertical direction for removing unwanted substances from the supporting semiconductor. This shows efficacy of etching procedure of proposed system than other conventional etching processes.

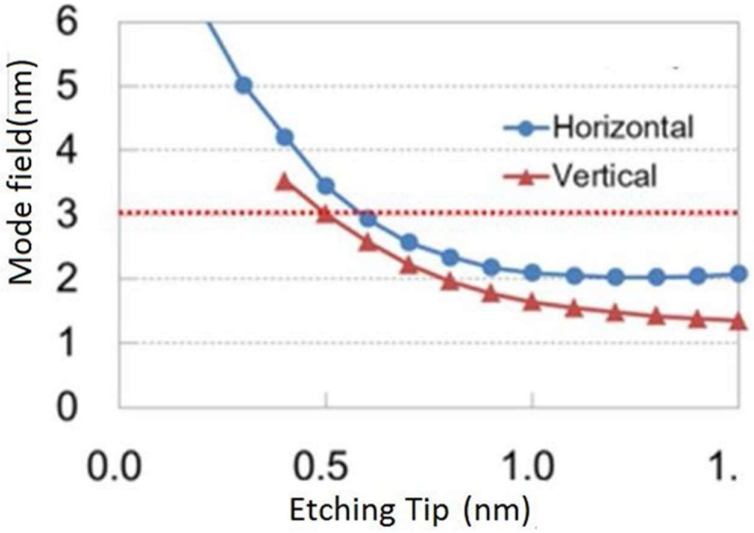

Figure 7. Representation of even cross-sectional etching process

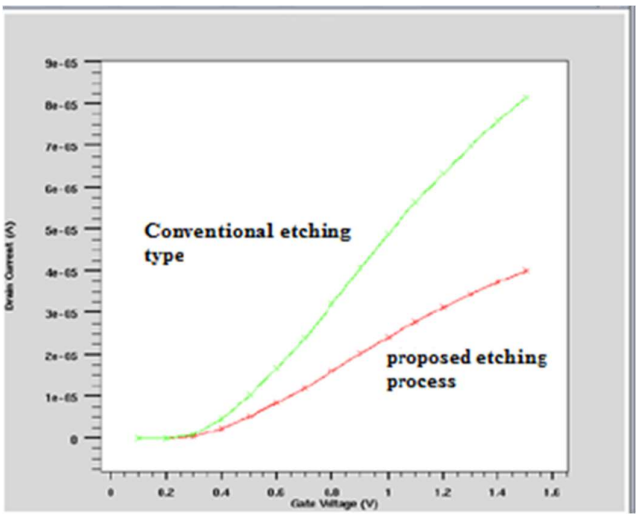

Figure 8. Representation of current- Leakage of etching process

In general current- leakage in GAAFET transistor makes the outer surface to accomplish a high temperature. This results in increasing of the surface temperature. Hence current leakage must be kept in control while transistor enters in to active region. As indicated in Figure 8, this is likely accomplished by the suggested thermal-based etching process as opposed to conventional etching procedures.

4. Advantages of thermal aluminum based etching methodology.

For the past decades there was a lack in research work in fabrication of chips. But in later 1990 many research studies methodology was proposed defined concentrated on the power dissipation of chips. Also, conventional technique will not suitable for nanometer scaled etching and fabrication processes. In the instance proposed system will suits for small scaled fabrication procedure and maintain its efficiency for both in increasing of etching cycles and high temperature. The major advantages of proposed system are described as below.

- Proposed system needs minimum time of exposure time of performing etching treatment on a semiconductor.
- It suits for three dimensional structures as it performs its etching process in cross sectional area.
- Maintain a stable surface temperature eve in increased number of etching cycles.
- It minimizes surface temperature in a faster manner than other conventional etching techniques.
- It suits for small scaled fabrication process.

5. Predictions and challenges.

Although thermal based etching procedure by usage of aluminum chemical components at the surface of semiconductor as a chemical film coating. The process is a temperature sensitive procedure. It is difficult to maintain the surface temperature in constant manner on whole fabrication processes.

It is any temperature change in surface may leads to ionic-reaction on the surface, physical damages on semiconductor. This is to be big challengeable parameters in fabrication steps. It was not maintained in a stable manner for all of the conventional etching treatment methodology. But in the instance, proposed type of etching maintains a stable temperature even in increases of etching cycles.

6. Conclusion and stance of proposed system.

A perfect Etching process can potentially reduce leakage current in a FET. The extent to which it does so, however, depends on the specific etching method used. For example, dry etching can create a rough surface that may increase leakage current, while wet etching can create a smoother surface that may decrease leakage current.

In conventional etching procedures temperature of outer surface is concentrated on forthcoming fabrication processes. This leads to power dissipation from the etched area, unwanted ionic reaction on the semiconductor surface. Hence it is vital to describe a sustainable chemical based etching procedure which can able to sustain high temperature and lowered its surface temperature of semiconductor on completion of etching treatment. The proposed system proves its sustainability of high temperature (say 300’c) and minimizing surface temperature in faster manner on comparison of other conventional etching procedure. It is concluded that ALE based etching can potentially decrease short channel effect in a FET and reduce leakage current depending on the specific etching method used and the properties of the FET itself.

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