Journal of Data Acquisition and Processing
ISSN: 1004-9037
https://sjcjycl.cn/
DOI: 10.5281/zenodo.7922866

LOW TRANSITION ACCURACY CONFIGURABLE RADIX 4 ADDER

R.Devadharshini[1], Dr.S.Bhavani[2] , Dr.Gnanasaravanan Subramaniam[3] ,R.Sudha[4]
[1],PG Scholar, Department of Electronics & Communication. Sri Shakthi Institute of Engineering & Technology, Coimbatore, India.
[2],Professor,Department of Electronics & Communication.Sri Shakthi Institute of Engineering & Technology, Coimbatore,India.
[3],Assistant Professor, Department of Biomedical Engineering.Karunya Institute of Technology and Sciences,Coimbatore,India.
[4]Associate Professor,Department of Electronics & Communication. Sri Shakthi Institute of Engineering & Technology,Coimbatore,India.
r.devadharshini99@gmail.com,hodece@siet.ac.in,
gnanasaravanan@gmail.com,r.sudha@siet.ac.in

ABSTRACT: Approximate computing can successfully attain lower computational costs. The computational accuracy and the circuit's size, delay, and power requirements are traded off in this method. However, the accuracy standards may vary depending on the application. In some situations, accurate results are required. In order to compute accurate or approximative results, this work proposes a low transition accuracy-configurable radix-4 adder (ACRA) that makes advantage of the power gating mechanism. To evaluate whether the MSP influences the calculation outcomes in the bipartitioned low transition, a detection-logic unit must be used to detect the effective input ranges. In an effort to narrow the discrepancy between the approximate and accurate findings, the partial sum of one adder element is altered while the ACRA operates in the approximate mode. ACRA obtained the best power-delay product/computational accuracy trade-off when compared to two state-of-the- art accuracy adjustable adders. In low transition, the input data are blocked by a data latch, the correct sign signals are corrected using a SE unit, and the effective ranges of the input data are determined using an ACRA detection-logic unit. The power consumption and delay could be decreased by up to 25% to 30% with the suggested low transition ACRA.

Keywords - Accuracy-configurable, approximate computing, image quality, radix-4 adder, detection logic, sign extension.

1. INTRODUCTION

In recent years, approximate computing has gained popularity as a computer technique. Approximate circuits are digital circuits that are built in such a way that the functional requirements are not met and some space, energy, or time savings are needed. The fundamental concept is to trade accuracy for energy consumption by utilising the system's built-in error resilience or mistake tolerance to achieve energy efficiency. In most circumstances, a trade-off like this is also connected to performance enhancements like quicker operations, area reduction, etc.

If a circuit in an application has flaws that could lead to internal and external mistakes and the system it is a part of generates good results, the circuit is said to be error-tolerant (ET). To produce approximations, ETAI is split into an accurate portion and an inaccurate portion. To speed up the adder, ETAII reduces carry propagation, and ETAIIM modifies ETAII by linking carry chains in precise MSB sections. Although the ET circuit may result in incorrect outputs, it is nonetheless used because it increases effective yield, boosts revenues, and uses less expensive parts [3]. It can be thought of as a new trade-off factor in addition to power and speed.

Many established and new application fields, including multimedia processing, wireless communications, networking, recognition, mining, and synthesis, exhibit the trait of intrinsic resistance to "errors" made during their implementation. This resilience is a result of a number of variables, including (i) the frequent processing of big data sets with high redundancy, (ii) the use of statistical or probabilistic computations, and (iii) the inability of humans to detect even a little amount of mistake in outputs. Circuits can run with "zero margins" even when there are process, voltage, and temperature changes thanks to a similar class of approaches [5], [6] that rely on detection, followed by correction or prediction, followed by multicycle operation, respectively, to prevent timing errors..

In order to achieve energy efficiency, the majority of these systems use voltage over scaling (VOS), where the voltage is scaled to a point where some of the logic's routes' delays surpass the clock period, hence creating "errors". We examine typical computational kernels used in multimedia, recognition, and mining algorithms and suggest design strategies to improve the hardware implementations of these meta functions VOS behaviour, i.e., reduce the number of mistakes they produce. The following are the main contributions of this work: to recognise the computing cores in representative multimedia, recognition, and mining algorithms and to examine how they behave under VOS. To take into account coarse-grained meta-functions that are iteratively run across a number of cycles, as they make some of the suggested design strategies possible. We analyse the advantages of the suggested design techniques and also show how optimizations at the meta-function level translate into advantages at the application level in terms of improved energy vs. output quality tradeoffs. This is done using a combination of transistor-level simulation and system- level simulation.

An n-bit adder is split up into a number of smaller, autonomous block adders using the CSPA. To anticipate the carry-out bit, each block adder has its own carry predictor circuit. In order to decrease the critical path time, CSPA also isolates the carry and sum generator circuits. A Variable Latency Carry Speculative Adder (VLCSPA) is created by adding error detection and recovery circuits to the CSPA. Therefore, in this work, we focus on implementations of error-tolerant applications like image and video compression that are application-specific integrated circuits. We focus on the computationally demanding blocks in these applications and construct them with approximative hardware to demonstrate significant reductions in power usage with minimal output quality degradation.

2. SYSTEM IMPLEMENTATION

2.1RD4A

In comparison to a conventional adder, the RD4A uses less power and propagates data at twice the speed. There are two categories of design techniques for an accuracy-adjustable adder: methods based on carry prediction and methods based on error correction. A number of overlapping sub adders that are utilised for error detection and correction are added to an approximation adder to increase its accuracy. To gradually rectify the computing result, the error correction process is carried out from the Least Significant Bit (LSB) to the Most Significant Bit (MSB).

2.2 ACCURACY-CONFIGURABLE RD4A

The ACRA has two modes of operation: the approximate mode, which uses it as a approximate adder, and the exact mode, which uses it as a normal adder. The basic technique of the proposed ACRA for changing the computational precision is power gating technology.

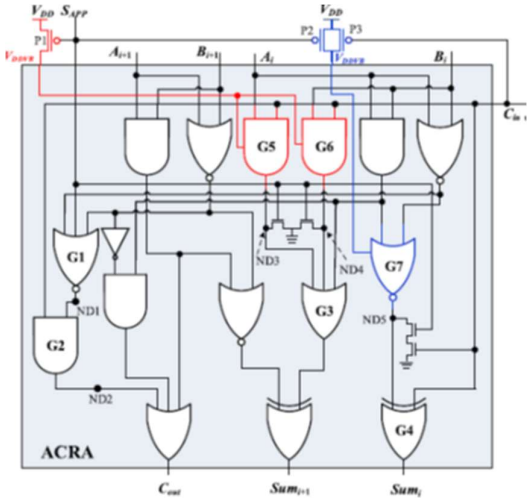

Figure 1 ACRA

Figure.1 depicts the ACRA, with G5–G7 being controlled by power gating under various circumstances, and the other logic gates being always-on logics. ACRA operation mode is controlled by the input signal SAPP in Figure.1, which is a control signal. The ACRA functions in two modes: approximation mode when SAPP is 1 and exact mode when SAPP is 0. The top portion of the diagram shows the ACRA's power source. When the ACRA performs approximate computations, G1 and G2 stop their internal signal-switching activities,which reduces power consumption.

2.3 LOW TRANSITION ACRA:

In addition to explanations presented in previous studies, this paper provides a further explanation of the proposed low-transition ACRA. To explain the reason for these low-signal transitions, let's examine five cases of 16-bit addition. Swapping operands A and B in an addition results in the same low transition. So, based on this design, there are probably no more than these five. In such cases, the results of MSP are predictable. Therefore the computation in MSP is useless and can be ignored. To know if MSP affects the calculation result of the two-

part low transition method, the valid input range should be detected using the detection logic unit.

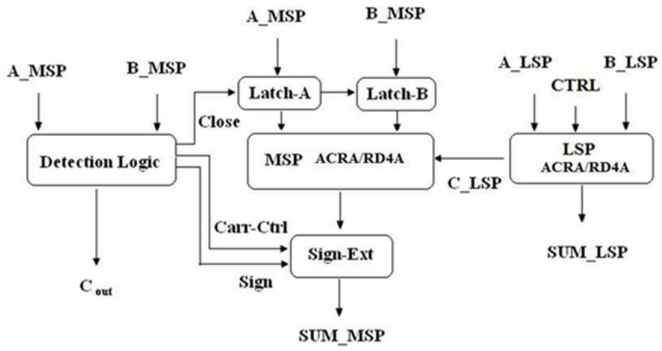

Figure 2. Block diagram of Low transition 8bit ACRA.

The 8-bit adder is divided into MSP and LSP at the 4th and 5th bits. A latch implemented by a simple AND gate is used to control the MSP's input data. If MSP is required, the input data for MSP is not changed. However, if the MSP is negligible, the input data to the MSP will be zero to avoid power consumption due to glitches. With the exception of the adder, the two operands of MSP enter a detection logic unit that can decide whether to turn off MSP.

Close, one of the detection-logic unit's three outputs, indicates whether or not the MSP circuits can be overlooked. The value of close becomes 0 when the two input operands can be categorised into one of the five scenarios, indicating that the MSP circuits can be closed to reduce power consumption. By manipulating the three 1-bit registers at the detection-logic unit's outputs, a specific amount of delay is employed to assert the close, sign, and carry-ctrl signals after the period of data transfer.

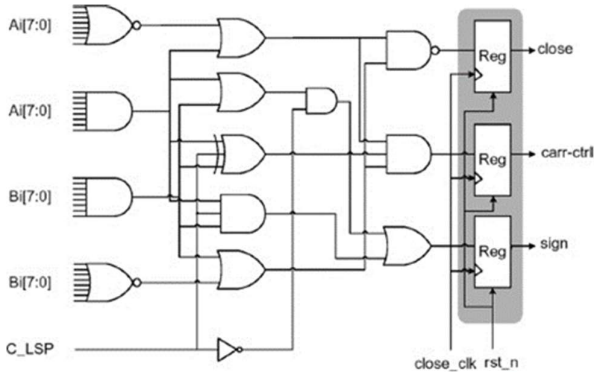

Figure 3. Detection-logic unit

Since the MSP outputs are instantly compensated by the SE unit, the time saved by avoiding the computations in the MSP circuits shall cancel out the delay caused by the detection-logic unit when the MSP is turned off by the detection-logic unit. Before turning on the data latches in the MSP so that data can enter, the circuits in the detection-logic unit must wait for notice. The SE circuits can be easily built by multiplexers to account for the MSP's sign signals. Pseudo summations (PS) from the MSP adder/subtractors serve as the input data for the SE circuits.

2.4 SOFTWARE DESCRIPTION

A Hardware Description Language (HDL) is Verilog. A language used to describe a digital system is known as a hardware description language. The design can be entered using graphical schematics, state machine diagrams, VHDL, and Verilog thanks to the Xilinx ISE tools. All facts of the design flow are managed by the ISE® Design Suite.

3. RESULTS AND DISCUSSION

3.18BITACRA

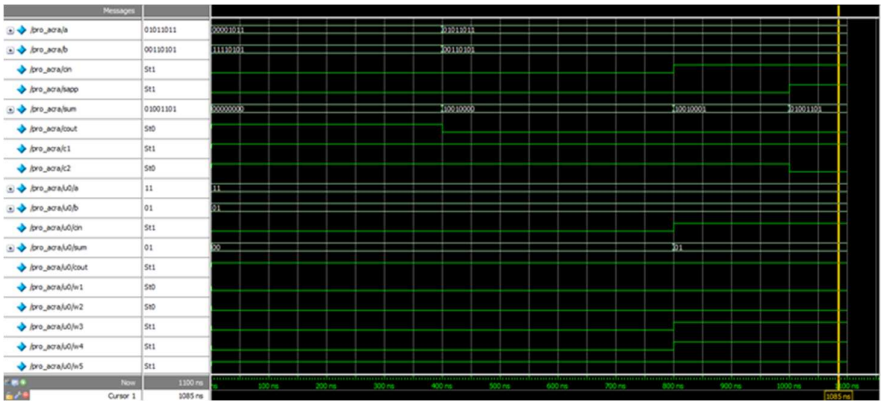

Figure: 4. Simulation result of 8 bit ACRA Adder

A and B is the 8-bit input of the proposed adder. CIN is the carry input an SAPP is the mode selection input. SUM is the output of the adder and COUT is the carry output. A single ACRA is a 2-bit adder. To implement a multibit adder, one RD4A and multiple ACRAs are added to an ACRA based completely configurable adder architecture. A total of n/2 adders are required for an n- bit completely configurable adder. Only the lowest bit element is an RD4A, whereas the remaining n/2 − 1 adder elements are ACRAs.

3.2 LOW TRANSITION ACRA ADDER

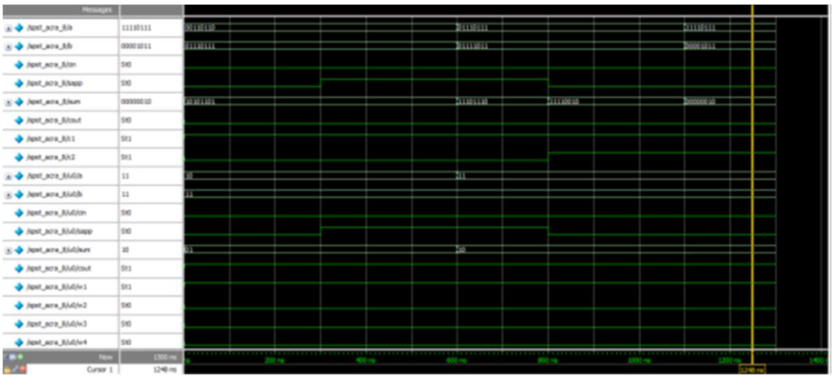

Figure: 5 Simulation result of 8 bit Low Transition ACRA Adder

A and B is the 8-bit input of the proposed adder. CIN is the carry input an SAPP is the mode selection input. SUM is the output of the adder and COUT is the carry output. A single ACRA is a 2- bit adder. To implement an 8-bit adder, pair of ACRAs is used in the LSP and another pair is used in MSP along with detection logic. Detection circuit along with latch and sign-extension block helps in minimizing the transition. A total of n/2 adders are required for an n-bit completely configurable adder.

3.3 COMPARISION

Parameters	LUT	Delay(us)	Power(mW)
ACRA	16	18.457	506
Low Transition ACRA	24	16.446	475

Table :1 Comparision between ACRA & Low Transition ACRA

4. CONCLUSION

It is suggested to use an ACRA to change the computational accuracy between accurate and approximate mode. The ACRA obtained about the same results in the approximate mode as it did in an accurate operation, but it had a 45%–80% lower PDP than a traditional RCA. The theoretical analysis and implementation concerns of the Low Transition ACRA are thoroughly covered as the Low Transition ACRA explores its applications in multimedia/DSP computations. The switching (or dynamic) power dissipation, which makes up a sizable amount of the total power dissipation, can definitely be reduced by the suggested Low Transition ACRA. As a result, the power and delay are reduced by 25% to 30% by the suggested Low Transition ACRA.

REFERENCES

[1] F. Frustaci, S. Perri, P. Corsonello, and M. Alioto, "Energy-quality scalable adders based on nonzeroing bit truncation," IEEE Trans. vol. 27, no. 4, pp. 964–968, Apr. 2019.

[2] M. Biasielli, L. Cassano, and A. Miele, "An approximation-based fault detection scheme for image processing applications," in Proc. Design, Autom. Mar. 2020, pp. 1331–1334.

[3] L. Jin and H. Liang, "Deep learning for underwater image recognition in small sample size situations," in Proc. OCEANS Aberdeen, Jun. 2017, pp. 1–4.

[4] Y.-J. Chang,Y.-C .Cheng, Y.-F.Lin ,S.-C. Liao, C.-H.Lai, and T.-C.Wu, "Imprecise 4-2 compressor design used in image processing applications," IET Circuits, vol. 13, no. 6, pp. 848–856, 2019.

[5] S. Natarajan, Imprecise and Approximate Computation, vol. 318. New York, NY, USA: Springer, 1995.

[6] G. Paim, L. M. G. Rocha, G. M. Santana, L. B. Soares, E. A. C. da Costa, and S. Bampi, "Power-, area-, and compressionefficient eight-point approximate 2-D discrete Tchebichef transform hardware design combining truncation pruning and efficient transposition buffers," IEEE Trans.. Papers, vol. 66, no. 2, pp. 680–693, Feb. 2019.

[7] Z. Zhang, Y. He, and B. Zhang, "A time-efficient automatic circuit approximation method," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 67, no. 9, pp. 3047–3055, Sep. 2020,

[8] M. Ramasamy, G. Narmadha, and S. Deivasigamani, "Carry based approximate full adder for low power approximate computing," in Proc. 7th Int. Conf. Smart Comput. Commun. (ICSCC), Jun. 2019, pp. 1–4. 58

[9] N. Van Toan and J.-G. Lee, "FPGA-based multi-level approximate multipliers for high-performance error-resilient applications," IEEE Access, vol. 8, pp. 25481–25497, 2020.

[10] N.-C. Huang, S.-Y. Chen, and K.-C. Wu, “Sensor-based approximate adder design for accelerating error-tolerant and deep-learning applications,” in Proc. Design, Autom. Test Eur. Conf. Exhib. (DATE), Mar. 2019, pp. 692–697.