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DESIGN AND IMPLEMENTATION OF D FLIP-FLOP FOR AREA EFFICIENT, LOW POWER APPLICATIONS USING MGDI TECHNIQUE

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Abstract: After the emerge of VLSI in this world, it had made the innovation to grow at faster rate. VLSI chiefly centres around lessening the number of transistors, area, power and delay which are the major standards of it. These factors improve the VLSI products to be cost effective, highly reliable, improved performance and increases the operating speed with less power. USR has various applications like memory blocks in PC's, serial and parallel data transfer and data converters, micro-controllers etc. In this paper, the idea of reduced area, low power and less delay is presented with m-GDI technique. This paper is based on designing the front-end and back-end of 8-bit USR using m-GDI technique in cadence virtuoso tool utilizing gpdk45 library. The examination table of area, power and delay using m-GDI, GDI and CMOS technique is also illustrated.

Keywords: Modified Gate Diffusion Input, 8-bit USR, area, power, delay, transistor, layout, cadence, virtuoso tool, gpdk45 library, CMOS technology.

1. INTRODUCTION

a) CMOS Technology

The primary motive for developing the complementary MOSFETs (CMOS) technology was achieving high speed in logic gates for digital circuits, with low power dissipation. CMOS makes possible the production of numerous potent analog and digital circuit configurations. CMOS is similar to BJT logic devices but switched by voltage rather than current – no current flows into the gate of a CMOS. Complementary MOS, or CMOS, is ubiquitous in digital circuits, becoming the preferred technology for complex digital integrated circuits. Complementary means that the transistors operate in pairs, one NMOS and one PMOS in the same chip – both are enhancement MOSFETs. A turned-on transistor has a low resistance between source and drain. In contrast, the resistance is high when turned off. A CMOS inverter

uses one NMOS transistor and one PMOS transistor connected in series. The PMOS attaches to the power supply +V and the NMOS to the ground. When the input is logic 0 the NMOS transistor is off, and the PMOS transistor is on. The output is pulled up to logic 1 because it is connected to +V but not to the ground. With a logic 1 input, the NMOS is on, the PMOS is off, and the output is pulled down to logic 0. Like any other FET device, a CMOS has insulated input gates. Therefore, the input current is very low.

b) GDI technology

Gate diffusion input (GDI) - a new technique of low-power digital combinatorial circuit design. This technique allows reducing power consumption, propagation delay, and area of digital circuits while maintaining low complexity of logic design. GDI stands for Gate Diffusion Input Technique. Fig.1 shows the basic GDI cell.

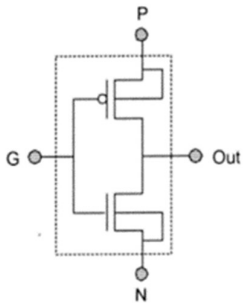

Fig.1 GDI cell

It has three input terminals

- G- common gate input of NMOS and PMOS
- P- input to the source/drain of PMOS
- N- input to the source/drain of NMOS

The bulk terminal of PMOS and NMOS are connected to the P and N terminals respectively. Comparing to CMOS, it consumes only less power. Since the circuit design is low complex, it requires only less area. Though GDI technique is more advantageous compared to CMOS, it has its own drawbacks. GDI faces difficulty in obtaining strong 0 and strong 1 at the output for certain combinations of input. It is difficult to manufacture in macro scale. The output voltage drop will get degraded and causes overuse of power consumption. The bulks of NMOS and PMOS are constantly connected to VDD and GND respectively which also results in high power consumption.

c) m-GDI technology

m-GDI technique m-GDI stands for modified Gate Diffusion Input technique. The PMOS transistor bulk node is connected to the VDD which is referred as the high constant voltage. The NMOS transistor bulk node is connected to the GND which is referred as the low constant voltage. Fig.2 shows the complete structure of m-GDI cell.

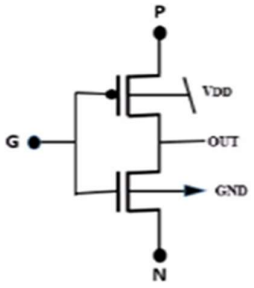

Fig.2 m-GDI cell

Since the silicon area is very much reduced compared to other conventional methods, the top down design approach is very simple and easy. The leakage power and the switching power have been lowered. Due to these properties, it consumes less power and delivers high speed.

d) Universal Shift Register (USR)

In digital electronics, shift registers are the sequential logic circuits that can store the data temporarily and provides the data transfer towards its output device for every clock pulse. 8-bit Universal Shift Register is shown in Fig.3. These are capable of transferring/shifting the data either towards the right or left in serial and parallel modes. Based on the mode of input/output operations, shift registers can be used as a serial-in-parallel-out shift register, serial-in-serial-out shift register, parallel-in-parallel-out shift register, parallel-in-parallel-out shift register.

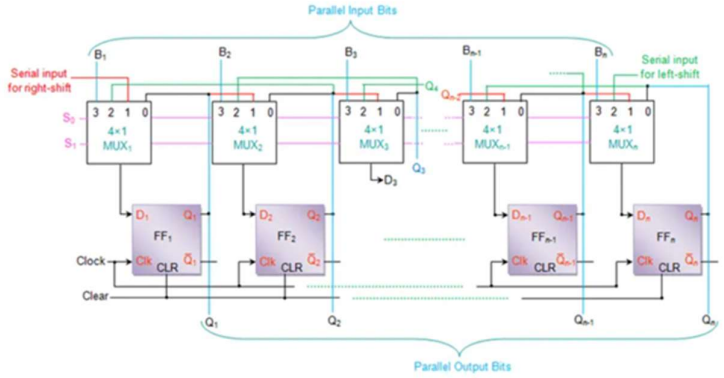

Fig.3 8-bit Universal Shift Register

A register that can store the data and shifts the data towards the right and left along with the parallel load capability is known as a universal shift register. It can be used to perform input/output operations in both serial and parallel modes. Unidirectional shift registers and bidirectional shift registers are combined together to get the design of the universal shift register. It is also known as a parallel-in-parallel-out shift register or shift register with the parallel load.

e) Tools used:

Cadence is a leading software platform for designing and verifying complex digital, analog, and mixed-signal integrated circuits and micro-electromechanical systems. Cadence offers a comprehensive suite of tools that allow you to design, verify, and implement cutting-edge VLSI projects. From schematic capture and simulation to routing and place and route, cadence has everything you need to bring your projects.

LVS stands for Layout Vs Schematic. It is one of the steps of physical verification; the other one being DRC (Design Rule Check). While DRC only checks for certain layout rules to ensure the design will be manufactured reliably, functional correctness of the design is ensured by LVS.

2. DESIGN METHODOLOGY

a) Universal Shift Register (USR)

USR is a shift register which can be operated in all modes. USR can have a number of modes to operate it. In my case we designed it for two control lines which can be operated in four modes. For control lines s0s1=00 no change or output of USR always keep the previous value. Similarly s0s1=01 give left shift, s0s1=10 right shift and s0s1=11 parallel load. The design of USR consists of D F-F and mux. D F-F is designed with the help of NAND and NOT gates. Fig.4 and Fig.5 shows the Schematic design and layout of Universal Shift Register respectively.

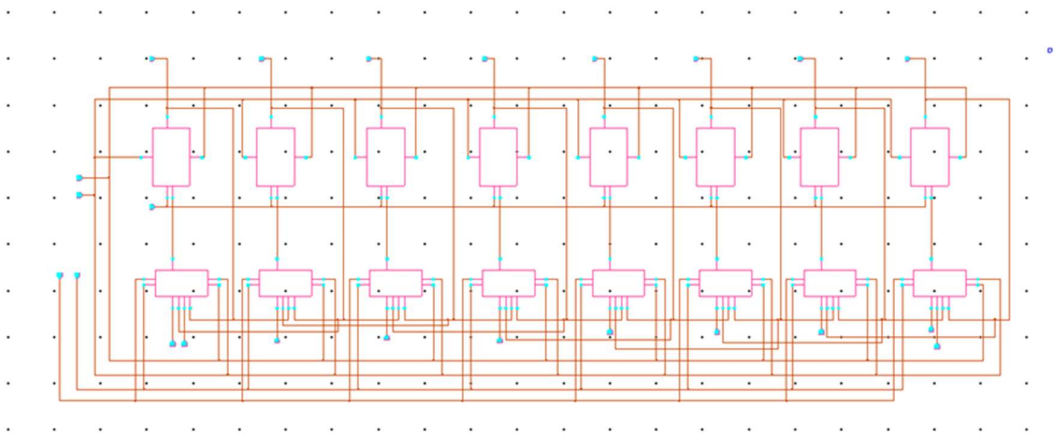

Fig.4 Schematic of Universal Shift Register

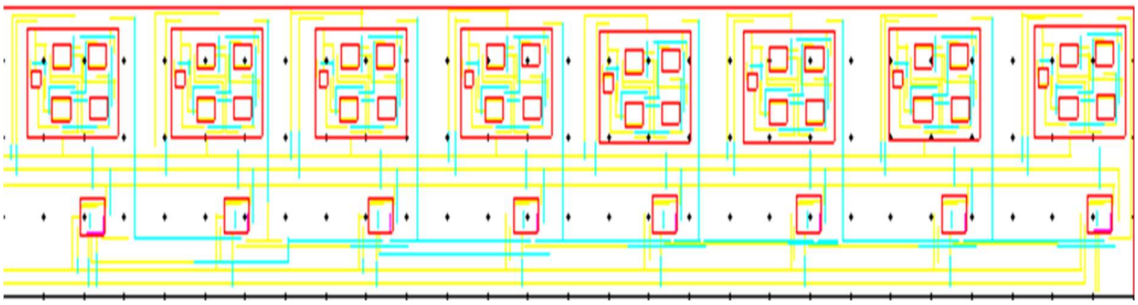

Fig.5 Layout of Universal Shift Register

b) 4:1 Multiplexer

Multiplexer is a combinational circuit that has maximum of 2n data inputs, ‘n’ selection lines and single output line. One of these data inputs will be connected to the output based on the values of selection lines. Since there are ‘n’ selection lines, there will be 2n possible combinations of zeros and ones. So, each combination will select only one data input. Multiplexer is also called as Mux. 4x1 Multiplexer has four data inputs 3, 2, 1 & 0, two selection lines s1 & s0 and one output Y. The schematic design and layout of 4:1 mux is shown in the following Fig.6 and Fig.7 respectively.

Now, there will be 4 cases as described below:-

- When the selection line s0, s1 represents 00, mux will be short circuit for input line 0 and will be open circuited for other input lines.
- When the selection line s0, s1 represents 01, mux will be short circuit for input line 2 and will be open circuited for other input lines.
- When the selection line s0, s1 represents 10, mux will be short circuit for input line 1 and will be open circuited for other input lines.
- When the selection line s0, s1 represents 11, mux will be short circuit for input line 3 and will be open circuited for other input lines.

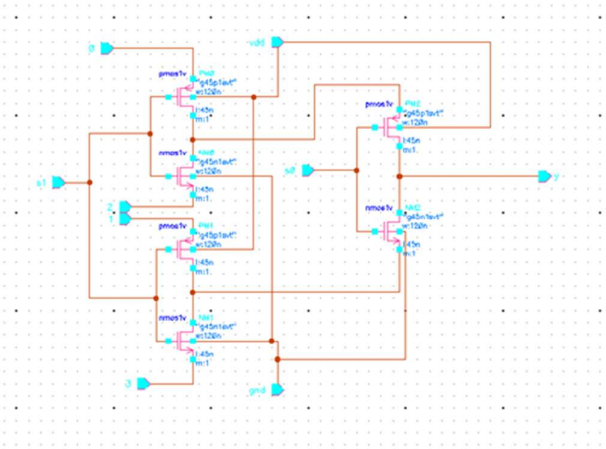

Fig 6. Schematic design of 4:1 mux

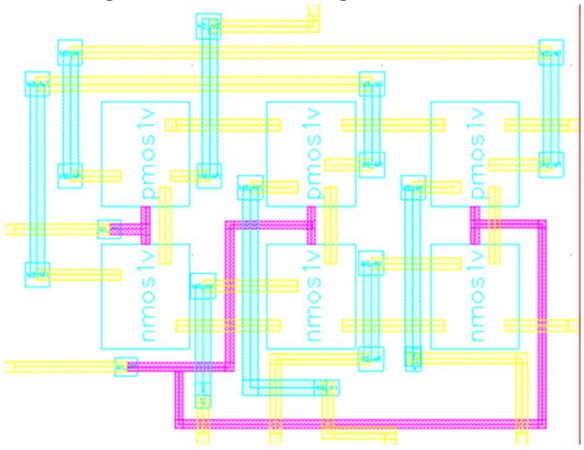

Fig 7. Layout of 4:1 mux

c) D FF

The D flip-flop is a two-input flip-flop. The inputs are the data (D) input and a clock (CLK) input. The clock is a timing pulse generated by the equipment to control operations. The D flip-flop is used to store data at a predetermined time and hold it until it is needed. This circuit is sometimes called a delay flip-flop. In other words, the data input is delayed up to one clock pulse before it is seen in the output.

There are 2 cases in D FF

- When clk = 0; d ff will stay idle in its state.
- When clk = 1; d ff starts to work by giving its input as output with a delay.

The schematic and layout of 4:1 d ff is shown in Fig.8 and Fig.9 and respectively.

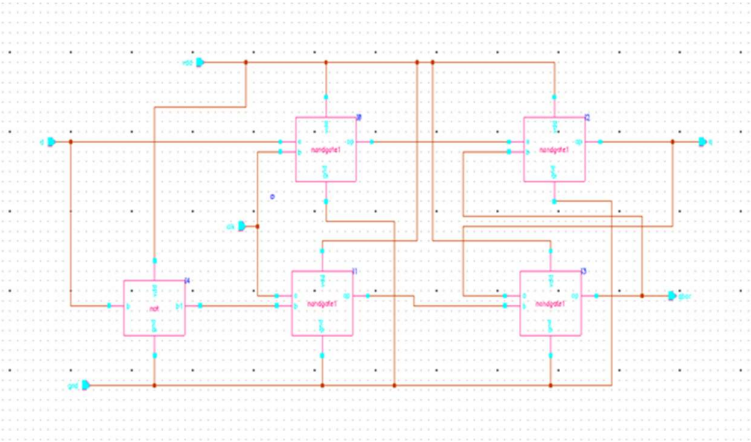

Fig.8 Schematic design of D FF

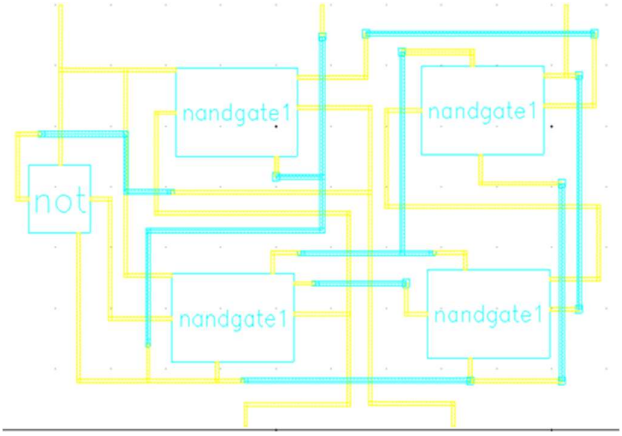

Fig.9 Layout of D FF

d) NAND Gate

A NAND Gate is a logical gate which is the opposite of an AND logic gate. It is a combination of AND and NOT gates and is a commonly used logic gate. It is considered as a "universal" gate in Boolean algebra as it is capable of producing all other logic gates. A NAND gate outputs a logical "0" for same combination of input – logic 1. The schematic and layout of nand gate is shown in Fig.10 and Fig.11 and respectively.

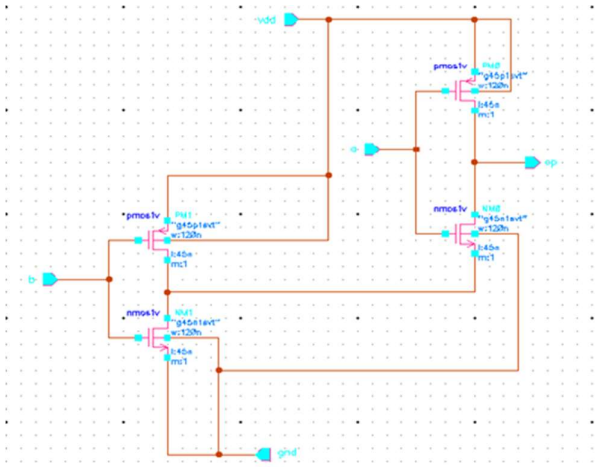

Fig.10 Schematic design of nand gate

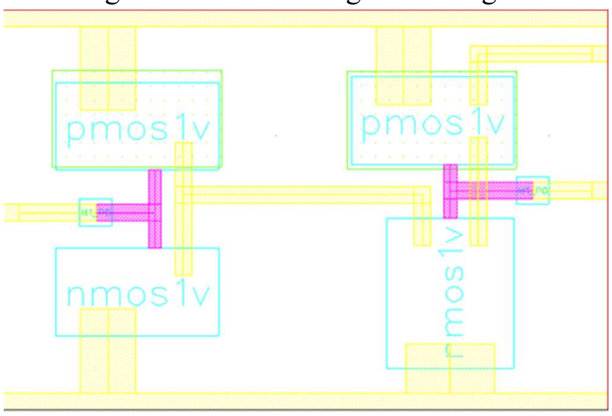

Fig.11 Layout of nand gate

e) NOT Gate

NOT gate is also called an inverter where it inverts the input signal that is applied to it. This is the single input and single output gate. Here, inversion corresponds that logic '0' to be converted into logic '1' and logic '1' converted to logic '0'. The schematic and layout of not gate is shown in Fig 12 and Fig.13 and respectively.

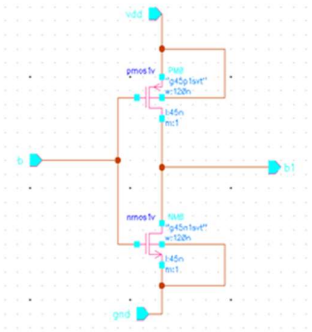

Fig.12 Schematic design of not gate

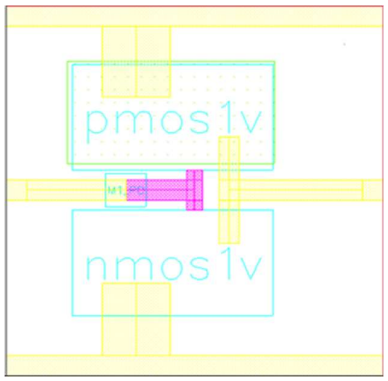

Fig.13 Layout of not gate

3. SIMULATIONS AND OUTPUTS

a) USR output

By giving the select lines s0s1 as 01 we enable the left shift pin and Fig.14 shows the output of the USR for the above mentioned condition.

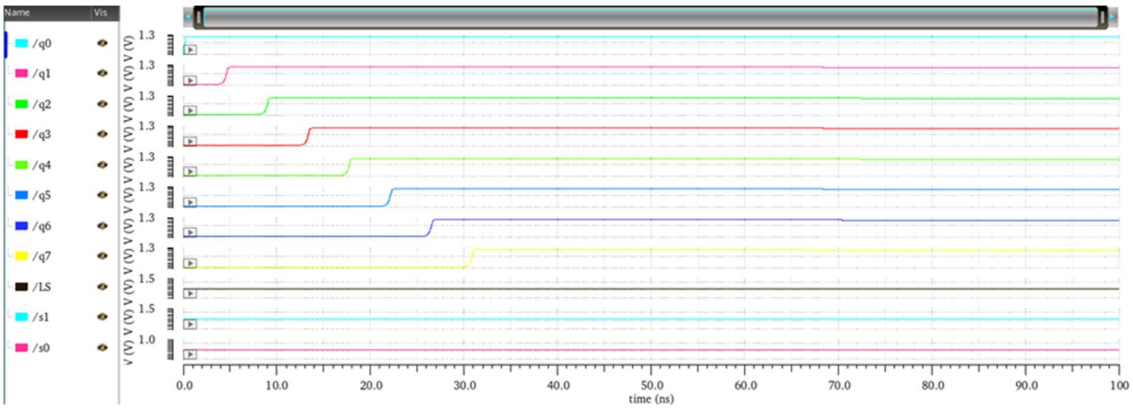

Fig.14 Left shift operation of 8-bit USR

By giving the select lines s0s1 as 10 we enable the left shift pin and Fig.15 shows the output of the USR for the above mentioned condition.

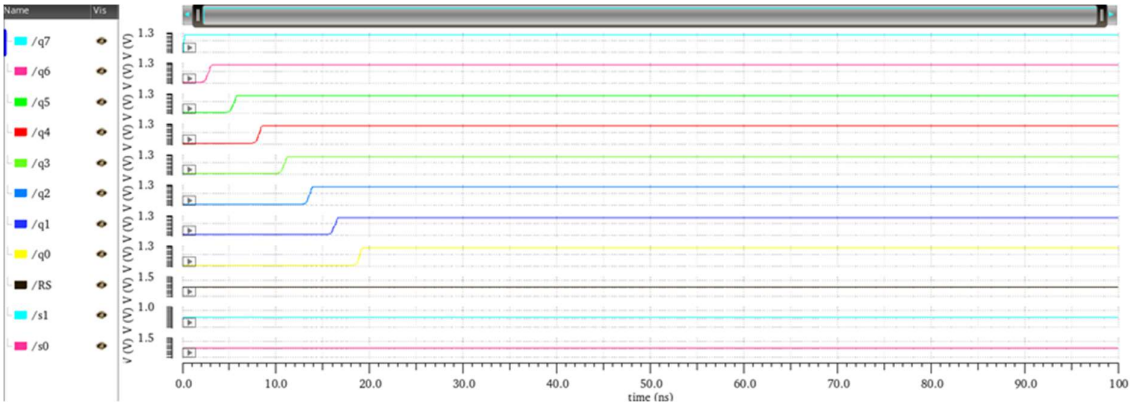

Fig.15 Right shift operation of 8-bit USR

Design Rule Check (DRC) verifies as to whether a specific design meets the constraints imposed by the process technology to be used for its manufacturing. DRC checking is an essential part of the physical design flow and ensures the design meets manufacturing requirements and will not result in a chip failure. The process technology rules are provided by process engineers and/or fabrication facility. The Fig.16 shows such DRC of 8-bit USR.

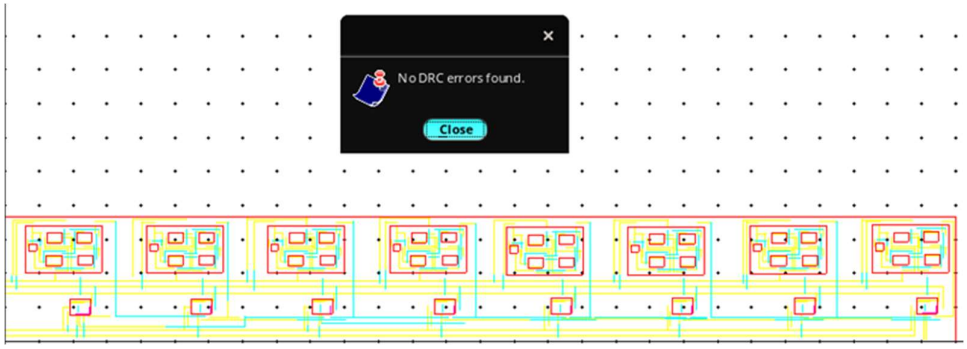

Fig.16 DRC output

Layout Versus Schematic (LVS) checking compares the extracted netlist from the layout to the original schematic netlist to determine if they match. The comparison check is considered clean if all the devices and nets of the schematic match the devices and the nets of the layout. Optionally, the device properties can also be compared to determine if they match within a certain tolerance. When properties are compared, all the properties must match as well to achieve a clean comparison. Fig.17 shows the LVS of 8-bit USR.

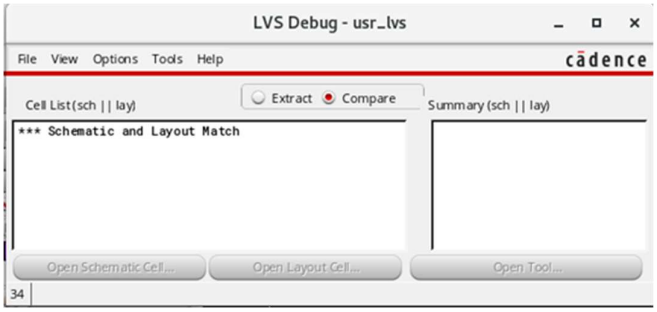

Fig.17 LVS check

b) MUX OUTPUT

Here from the Fig.18 we can observe that whenever both the select lines are high we get the output even if one of the select line is low output becomes low (ie) for the combination s0s1=11, we get output as in input 3 else 0.

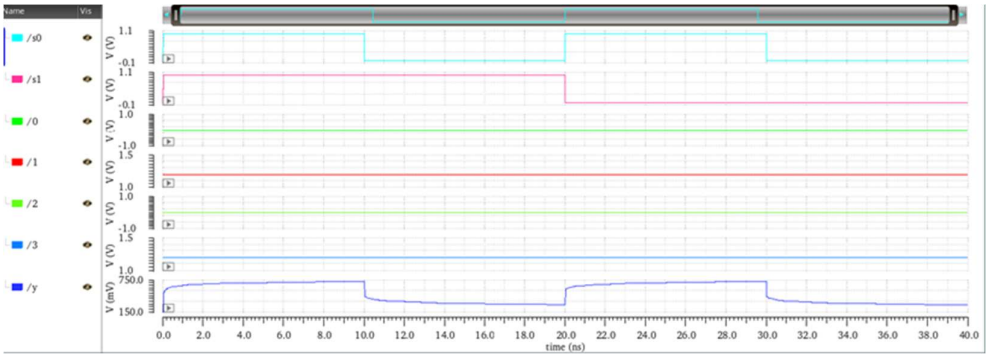

Fig.18 Output of 4:1 mux

c) D flip-flop

From Fig.19 it is clear that given input d is got as the output at q with clk trigger.

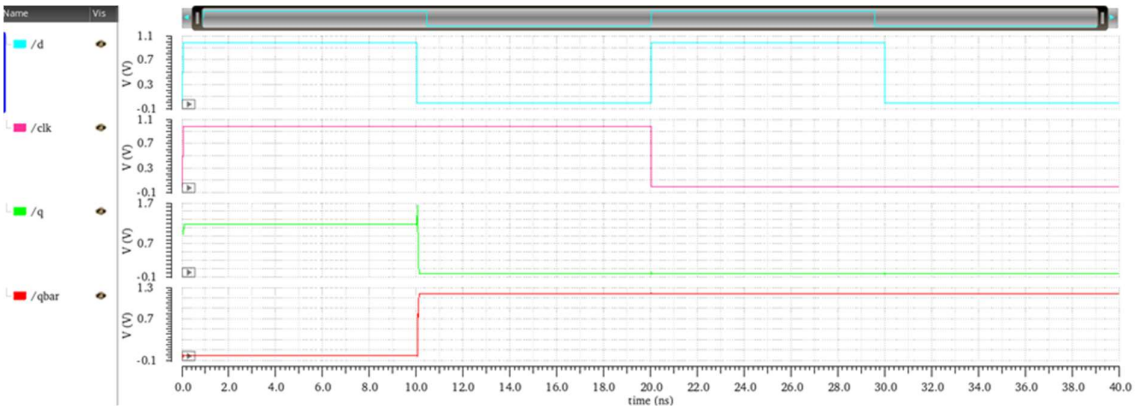

Fig.19 Output of d f-f

d) NAND GATE

For combination of inputs a = 1 and b = 1, output op = 0 and when inputs a = 0 and b = 0, output op = 1 as shown in Fig.20

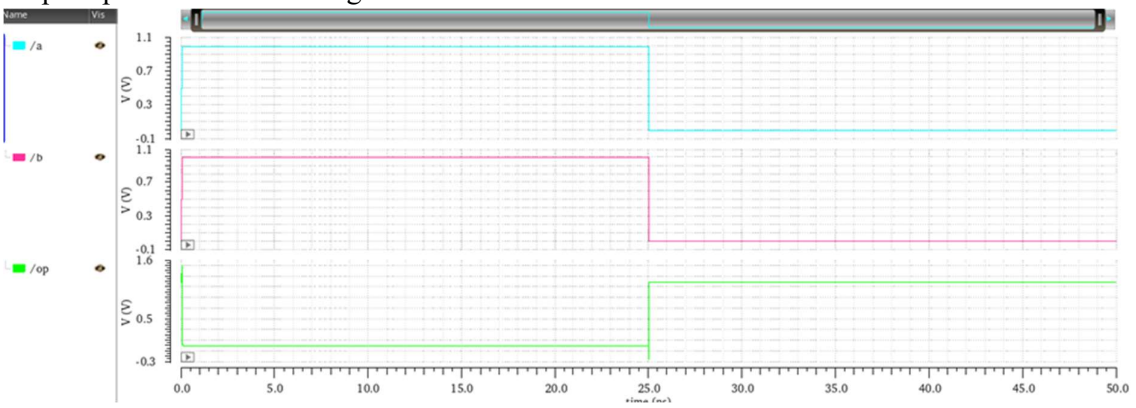

Fig.20 Nand gate output

e) NOT GATE

Not gate inverts the given input. From Fig.21 it is seen that the given input a is inverted and got as the output at y1.

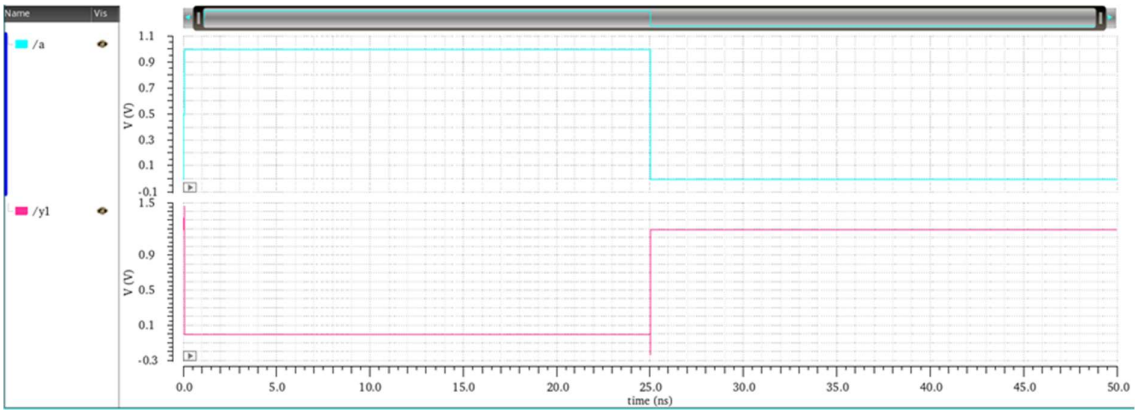

Fig.21 Not gate output

4. COMPARISON

The present innovation requests to create different new plan procedures to decrease the chip region, propagation delay and power utilization. So it is important to make examination against various innovative technologies. Table.1 gives the correlation against various innovations

where multi-inputs gate has carried out. This table essentially come up with plans to expand the outline by the utilization of TG, GDI and m-GDI technologies. In conclusion our design gives following outcome that is shown in table.1. TG tech utilizes 456 transistors while GDI tech utilizes just 312 transisters m-GDI tech utilizes just 192 transistors to execute the design (USR).

	NO OF TRANSISTERS	AVERAGE POWER	AVERAGE DELAY
CMOS	456	864.2µ	65.8 µs
GDI	312	633.8 µ	46.4 µs
m-GDI	192	9.43 µ	18.3 µs

5. CONCLUSION

In this paper low power and area efficient 8-bit universal shift register utilizing m-GDI technology is designed which is simulated using cadence virtuoso tool with gpdk045 library. The proposed universal shift register is having less number of transistors, power and delay than the other techniques. A performance comparison of the proposed 8-bit universal shift register is given using m-GDI, GDI and CMOS techniques. Therefore the proposed design has lower average power and lower area and is well suited for low power and high performance applications.

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