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A DUAL BOOST NINE-LEVEL INVERTER CIRCUIT FOR PV APPLICATIONS

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ABSTRACT: Integration of renewable energy with various power electronic inverters has been studied as a means of reducing reliance on fossil fuels. Due to its many benefits, multilayer inverters (MLIs) have become more popular in this context. In this paper, we suggest a new architecture that may enhance performance while using fewer parts. The suggested construction makes use of self-balancing capacitors that perform admirably regardless of load. It's important to note that even with the dual boost, the proposed circuit keeps the blocking voltage within the limits of the source voltage. Gating signals are obtained by a sinusoidal pulse width modulation switching approach. A simulation is carried out in MATLAB to assess the suggested inverter's effectiveness. The proposed circuit's potential advantages are also demonstrated by contrasting it with exchanged capacitor (SC)- based MLIs concerning the quantity of switches and standing voltage required.
Index Terms: Switched capacitor, nine-level inverter, PWM technique, and boost inverter.

1. INTRODUCTION

Systems for converting power, such as those used in electric vehicles, renewable energy, and STATCOM applications, rely heavily on multilayer inverters (MLIs) [1]. Multi-layer inductors are made up of a collection of power semiconductors such switches, diodes, capacitors, and dc sources. MLIs produce far less music, electromagnetic impedance, voltage stress, etc. than two-level inverters. MLI also offers additional benefits such flexibility, fault tolerant capabilities, dependability, minimal power loss, etc., and it delivers an excellent result with high productivity by elegantly combining various power components. These essential characteristics are why MLIs have recently become so popular in the academic world. Unlike the single-dc-source foundations of the capacitor-clamped MLI and the impartial point-cinched MLI, the ordinary flowed H-span MLI (CHB MLI) is made up of many independent dc sources. These MLIs need an extra voltage adjusting control circuit and a larger number of components since they generate several voltage steps at the output. Researchers have presented several strategies for optimising the size of the MLI, decreasing the total cost and unpredictability by reducing the amount of dc sources and power semiconductor gadgets, etc., as a result of its widespread use in industries, driving applications, photovoltaic (PV) systems, etc. These MLI topologies aim to minimise power loss, total standing voltage (TSV), and component count to improve overall efficiency [2]. In most cases, MLI will have a front-end dc level age circuit and a backside H-span to generate the necessary positive and negative voltages. Input voltage stress on H-bridge switches causes the TSV to rise when they are used. Nonetheless, H-bridge based designs are more common because of their versatility and expandability. But by carefully choosing the size of the dc sources used in the level production process, the MLI may be either symmetric or asymmetric. More levels may be accommodated by an asymmetrical structure,

whereas fewer controls are required for a symmetrical layout. In modern MLI topologies, a higher result voltage is one of the most significant features. Many other MLI topologies, all based on the SC method, have been created in the recent past, some of which use a single dc source while others use many sources. To increase the voltage's magnitude with no further inductors and transformers, switched-capacitor designs rely just on these two components: capacitors and semiconductors. By raising both the magnitude and the levels, capacitors enhance the waveform quality of the output signal. The SC MLI circuits' primary benefit is that the series-parallel voltage balancing approach may be used to achieve the necessary capacitor voltage without the need for any extra capacitor voltage balancing management. In [3], [4], and [5], a fundamental unit was created utilizing a back-end H-span. The voltage may be increased by a factor of four using the geography [3] with a solitary dc source, and this can be taken to an even greater extent for a greater total number of steps. This architecture employs fewer parts, but the H-bridge in the tail causes power to be distributed inequitably among the semiconductors. Another set of MLI topologies that may increase voltage from a single dc source are those described in [6], [7]. By carefully choosing the magnitude of numerous dc sources, this unit may be cascaded to generate very high voltages. Multiple-level output is possible from a single input using the generalised MLIs described in [8], [7], and this is verified at the nine-level setting. To account for TSV, the MLI described in [8] employs the high component but distributes the top voltage stress uniformly over every one of the switches. Using only 23 semiconductor switches, 6 diodes, and 6 capacitors, [9] demonstrates that a single dc arrangement can support 13 states. With only nine switches and a single capacitor, [10] verifies a five-level modular circuit. For each capacitor, the total boosting gain is 1, and the impeding voltage of all semiconductors is comparable to the data voltage. On the other hand, the higher the level cap, the more components are needed. In response to these issues, this work presents a simplified version of the conventional boost MLI that makes use of switching capacitors.

II.PROPOSED SYSTEM

The proposed system is a dual boost multilevel inverter circuit, and it uses a novel concept established in this study to boost the level using the reduced carrier PD-PWM approach, making it suitable for use in renewable energy applications. Based on the power or voltage level, execution, dependability, cost, and other specialized parameters, it is determined that the topologies are strongly tied to each individual application. A staircase voltage output waveform is synthesised using 13 semiconductor switches, 3 capacitors, and 1 dc source. A photovoltaic (PV) board, battery, or power module might act as the dc source. The terminals a and b are where the output voltage is measured. Using a series-parallel charging method, the voltage on the capacitor CB is raised to the inventory voltage Vdc. If you connect the capacitor in parallel to the source, it will charge, but if you connect it in series, it will discharge. Capacitor voltage is automatically maintained without any further regulation thanks to the CB 's inherent capacity to do so. The hindering voltage of the proposed circuit is well inside the allowable range for the source voltage. The supply voltage Vdc must be blocked by all switches except S8, which must block 0.5 Vdc. The general operation of the suggested nine-level circuit is shown in Fig. 2. In addition, the capacitor's maximum discharge and ripple voltage limits are taken into

account. The bare minimum capacitance that must be present (Cmin) regarding the most extreme release voltage, admissible wave voltage, is communicated as,

$$C_{min} = \frac{\triangle Q_{C_B}}{x\% \times V_{dc}} \qquad (1)$$

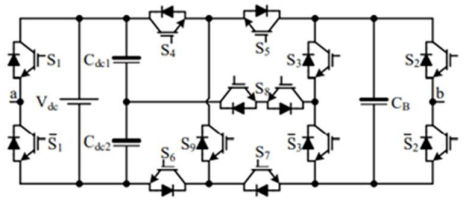

Fig.1: Dual-boost MLI circuit proposal

III.SYSTEM DESIGN AND IMPLEMENTATION

A. Description of a Circuit

In Fig. 1, we see a schematic portrayal of the proposed DB-MLI. It generates a 9-step staircase output voltage waveform using 13 semiconductor switches, 3 capacitors, and 1 dc source. Solar panels, batteries, or fuel cells may all be used as the dc source. Between a-b terminals, the output voltage is measured. Supply voltage is applied to capacitor CB. Vdc by using a series-parallel approach. A capacitor charges in parallel with its source and releases its stored charge when connected in series with it. The CB 's inherent capacity to regulate its own voltage means that no more regulation is required to keep the capacitor's voltage stable. The hindering voltage of the proposed circuit is well inside the extent of the source voltage, which deserves special note. The supply voltage Vdc must be blocked by all switches except S8, which must block 0.5V Vdc. The suggested nine-level circuit's precise operating principle is shown in Fig. 2. Capacitor seizure also takes the maximum discharge and ripple voltage into account. The discharge minimum capacitance (Cmin) is defined concerning the most extreme reasonable wave voltage, and is composed as,

$$C_{min} = \frac{\triangle Q_{C_B}}{x\% \times V_{dc}}$$

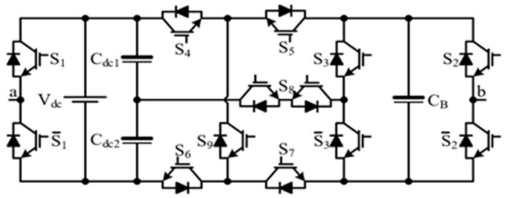

Fig. 1. Dual-boost MLI circuit proposal.

B. Modes of Operation

The voltage between the DC link and the boost capacitors is added to get the ideal result voltage. The Voltage Exchanging Table.

$V_o = V_{ab}$	Switches									Capacitor
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	C_B
$2V_{dc}$	1	0	1	0	1	1	0	0	1	D
$1.5V_{dc}$	1	0	1	0	0	0	0	1	0	D
$1V_{dc}$	1	0	1	1	1	1	1	0	0	C
$0.5V_{dc}$	1	1	1	0	0	0	0	1	0	-
0	1	1	1	1	1	1	1	0	0	C
0	0	0	0	1	1	1	1	0	0	C
$-0.5V_{dc}$	0	0	0	0	0	0	0	1	0	-
$-1V_{dc}$	0	1	0	1	1	1	1	0	0	C
$-1.5V_{dc}$	0	1	0	0	0	0	0	1	0	D
$-2V_{dc}$	0	1	0	1	0	0	1	0	1	D

Table I, we can see the proposed nine-level Db-Mli's table of switches.

Table I details the proposed DB-MLI's Vo =Vab level schema. Different modes of operation are displayed in Fig. 2 with the result voltage, Vo, and the current route via the active switches. Modes of operation during the positive half cycle are discussed below:

- S1, S¯2, S5, S6, and S9 are all active at a voltage of 2Vdc. A total of 2Vdc is generated at the a-b terminal by connecting a capacitor CB in series with the dc source.
- When the switches S1, S¯2, S3, S4 and S8 are all turned on and the voltage is set to 1.5Vdc, the CB will discharge to the load.
- The output voltage is 1Vdc when the switches S1, S¯2, S6, and S7 are all ON. Switches S4, and S5are used to charge capacitor CB at the same time.
- If switches S1, S¯2, S3, and S8 are all activated and Cf is charged, the resultant voltage at the output terminals is 0Vdc
- All switches S1, S2, S4, and S5 are active at a 0Vdc supply. Because there is now no voltage across the output because of the short between terminals a and b. By means of S6, and S7, capacitor CB is charged in parallel.

IV. MODULATION TECHNIQUE

Multilevel converters use a variety of modulation techniques to produce a sinusoidal flight of stairs yield waveform that consolidates central recurrence exchanging, space vector beat width tweak (SV-PWM), specific consonant end beat width balance (SHE-PWM), sinusoidal heartbeat width regulation (PWM), and other techniques [11], [12], [13], and [14]. As depicted in Figure, 3, the suggested inverter's operation is controlled utilizing the diminished transporter beat width tweak (PWM)method. It creates a four-stair waveform using a three-sided waveform (Vehicle 1 through Vehicle 4) and a corrected reference signal (Ref).The semiconductor switches are controlled by gate pulses derived from a comparison of carrier signals (P1 through P4) to a reference signal. A cycle selector, denoted by (C), may be used to distinguish positive and negative cycles. The balance file of the pinnacle amplitude.

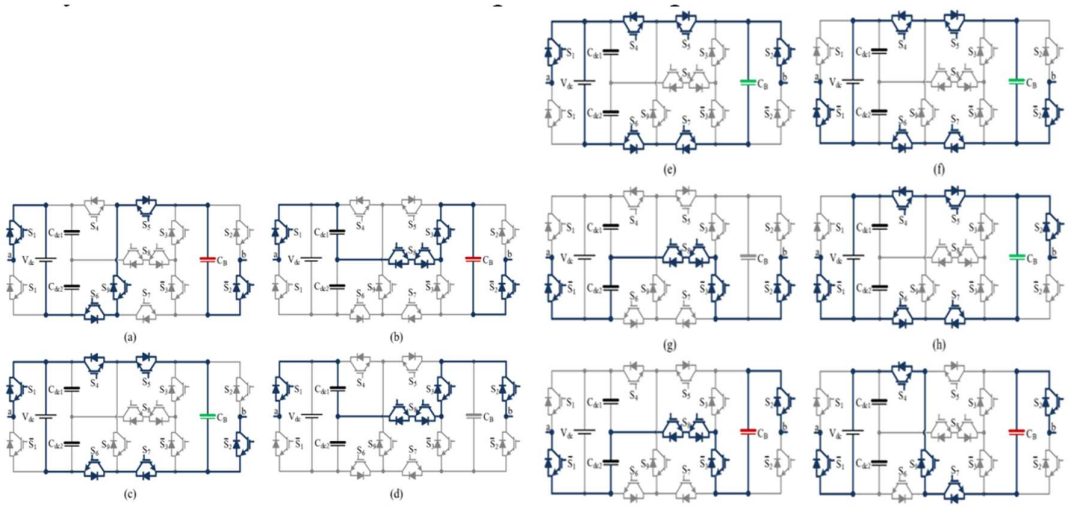

Fig. 2. Modes of operation: (a) $2V_{dc}$, (b) $1.5V_{dc}$, (c) $1V_{dc}$, (d) $0.5V_{dc}$, (e) $0V_{dc}$, (f) $0V_{dc}$, (g) $-0.5V_{dc}$, (h) $-1V_{dc}$, (i) $-1.5V_{dc}$, (j) $-2V_{dc}$.

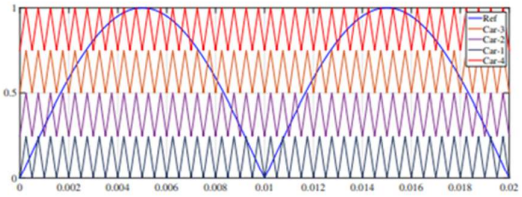

Figure 3: The Reduced Carrier Pd-Pwm Method

Magnitude reference (Vm), $(\widehat{V}_{Car})$
carrier waveforms is given by

$$m_a = \frac{V_m}{4 \times \widehat{V}_{Car}}$$

Therefore, the root-mean-square (RMS) of the air conditioner yield voltage might be determined in terms of the modulation index (ma) using the following formula:

$$V_{ab} \simeq m_a \frac{2V_{dc}}{\sqrt{2}}$$

To regulate the suggested circuit, we may construct the following general equations using logic gates:

$$S_1 = S_3 = C \quad (4)$$
$$S_2 = \bar{P}_2 \cdot C + P_2 \cdot \bar{C} \quad (5)$$
$$S_4 = S_7 = \bar{P}_1 + P_2 \cdot \bar{P}_3 + P_4 \cdot \bar{C} \quad (6)$$
$$S_5 = S_6 = P_4 \cdot C + \bar{P}_1 + P_2 \cdot \bar{P}_3 \quad (7)$$
$$S_8 = P_1 \cdot \bar{P}_2 + P_3 \cdot \bar{P}_4 \quad (8)$$
$$S_9 = P_4 \quad (9)$$

V.RESULTS AND DISCUSSIONS

Results

To ensure the created circuit would work, it is simulated in MATLAB/simulink. The 100 V dc supply is the active source. Three 1000 F capacitors are utilised in the circuit as a uninvolved source to keep CB at 100 V without utilizing a different voltage adjusting circuit. Exchanging happens at a pace of 2 kilohertz. The upsides of the not entirely set in stone by the longest possible discharging cycle, the maximum percentage of voltage ripple allowed, and a loading of Ω 30. Figure 4(a)(c) shows the simulation results under various loading circumstances. Figure 4(a) shows the voltages and waveforms produced by the capacitors under a load of 30 - 20 mH. The suggested circuit's capacity to increase voltage was shown using a nine-step load voltage ranging from 20 to 200 V in magnitude. The results of switching the load from 30 Ω - 20 mH to 60 Ω 40 mH are shown in Fig. 4(b). As the load value suddenly rises, a decrease in current greatness and a wave in capacitor voltage are expeditiously clear. In any case, the voltage is never changed all through the test. In Fig. 4(c), the outcome voltage stays undistorted even after a prompt change from no-store to full load. Regardless of what the load, the voltages across the capacitors and the significance of the fundamental parts of the result remain constant, as shown in Fig. 4(a)-(c). Due to the presence of a reverse flow channel for the current, the results verify the viability of the proposed MLI under strongly inductive loading. Therefore, both high and low power factor loads are acceptable. Additionally, the Fourier spectrum is shown in Fig. 5 and the overall harmonic distortion is claimed to be 13.51 percent at a modulation index of unity. The dominant harmonics are rearranged to the 39th and 41st orders as a result of the 2 kHz switching frequency. A quantitative correlation of the proposed circuit with as of late developed MLIs at the nine-level is also performed. The comparison between the established MLIs and the suggested MLIs for generating a certain voltage level is shown in Table II. The price of an MLI rises as more switches, diodes, and dc sources need to be used. The suggested MLI has reduced the number of switches significantly, with the exception of the circuit in [3], and subsequently, the exchanging misfortune is anticipated to be most reduced. H-span on the backside causes lopsided power circulation across the switches, though the geography in [3] utilizes less switches yet six diodes. To be clear, the suggested MLI is

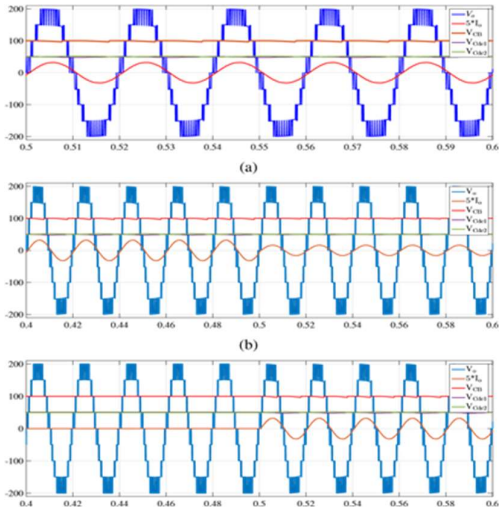

Fig. 4. Simulation results at: (a) 30 Ω - 20 mH load, (b) Step change in load from 30 Ω - 20 mH to 60 Ω - 40 mH, (c) No-load to full load condition.

VI.CONCLUSION AND FUTURE WORK

Conclusion

In this work, a novel nine-level DB-MLI has been proposed, and the operating principle is discussed in detail. Capacitors are smartly utilized to reduce the source count as well as to avoid the use of external voltage balancing control circuit. Thus, the proposed topology reduces the overall size and cost. Comparative assessment with the well-known MLI topologies shows the proposed topology utilizes fewer components for generating a particular voltage level. Simulation and analysis demonstrate the output voltage and capacitor voltages are maintained at the anticipated level regardless of the load value. Tests of a step-change in load validate the successive operation.

Future Work

Testing of the PV fed DB-MLI system with a suitable controller, and hardware implementation are the future works.

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