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DESIGN AND IMPLEMENTATION OF HYBRID FULL ADDER USING GDI FOR HIGH-PERFORMANCE APPLICATIONS

Y.E. Vasanth Kumar[1], K.P.Vinay[1] S. Bhuvana Chandra[2],S. Praneeth Kumar Reddy[3], S. Harish[4], T. Shiva Rama Krishna Reddy[5]

*1 Faculty, Dept of Electronics and Communication Engineering, Raghu Engineering College (Autonomous), Visakhapatnam, Andhra Pradesh, India

*2, 3, 4, 5 Student, Dept. of Electronics and Communication Engineering, Raghu Engineering College (Autonomous), Visakhapatnam, Andhra Pradesh, India

ABSTRACT

A full adder is a crucial part of designing many digital systems and it is utilised in many different applications, including digital signal processors, microprocessors, and microcontrollers. Electronic devices and circuits require great control, which calls for low power and high speed. The current paper serves as an example of the importance of power, delay, and transistor count in this context. In this paper a low power and high performance 1-bit full adder cell is implemented based on gate diffusion input (GDI). The delay, power, power delay product (PDP) are extracted and compared for the proposed full adder cell with other widely used full adders. For all varieties of full adders, we discover that the GDI approach effectively lowers power usage. However, compared to the CFA design, the MFA and HFA designs are slightly more delayed. The average power dissipation of proposed adder is about 83.2 pWatts at operational voltage of 1V. The next two adders which performed better are 12T and 10T GDI full adders with PDP of 2.7fj and 1.8fj. The proposed Hybrid Full Adder gives out lower PDP of 2.07aj than other adders. The performance of the proposed circuits was examined using Cadence Virtuoso tool at 1 V supply voltage with 45nm technology.

Key words: CMOS, Full Adder, Gate Diffusion Input (GDI), MGDI, Memory Cell.

1. INTRODUCTION

The foundation of many VLSI applications is based on logic gates such as AND, OR, XOR, and XNOR, which play a critical role in addition, subtraction, multiplication, and other operations. Adders are fundamental building blocks for digital systems, and their performance is essential in applications such as microprocessors, DSP, and image and video processing. As transistor density continues to double per square inch every year, researchers must prioritize chip area, speed, reliability, and low power consumption in adder design.

This study proposes using the gate diffusion input (GDI) logic to design AND, OR, XOR, and XNOR gates and compares the performance of two full adder design techniques. The conventional full adder (CFA), modified full adder (MFA), and hybrid full adder (HFA) are examined based on their power consumption, latency, and power-delay product. The results show that the GDI approach effectively reduces power consumption in both full adder designs compared to conventional CMOS and pass transistor logic designs. The MFA and HFA designs consume significantly less power than the CFA design, but they are slightly more delayed. However, the HFA design outperforms the alternatives in terms of power-delay product.

Overall, this study emphasizes the importance of balancing power consumption, latency, and transistor count in adder design. The GDI-based full adder designs offer a balance between power consumption and performance, demonstrating the potential for improving adder performance while reducing power consumption in VLSI applications. With the growing demand for low-power devices, researchers must continue to prioritize energy efficiency in digital system design, particularly in the development of adders that serve as fundamental building blocks for numerous operations.

2. GDI TECHNIQUE

The basic GDI cell is shown in Fig.1. It looks like CMOS inverter but the source and drain input of both the transistors are different.

In CMOS inverter, the source and drain inputs are always tied to VDD and GND respectively. While in GDI the diffusion terminal act as external input. GDI cell consist of three inputs.

1. G - it is input to both NMOS transistor and PMOS transistor.
2. P - it is input to the PMOS transistor.
3. N – it is input to the NMOS transistor.

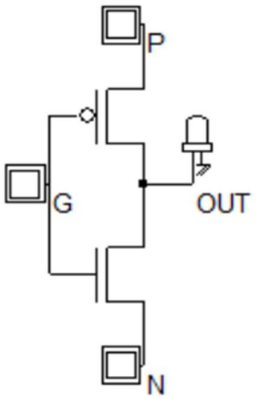

Figure 1: Basic GDI

It facilitates the realisation of the ions, including AND, OR, MUX, INVERTER, F1 and F2, as indicated in Table. 1

The implementation of several logic functions using the GDI approach is shown in Table 1. When these implementations are done with the help of CMOS then transistor count is increased and due to which the power consumption also increases while with the help of GDI, the transistor count is less, and power consumption is also low.

The relationship between input and output signals for each input combination is shown in the function table of a GDI model. It improves the performance of GDI circuit designs and ensures their accuracy. P- and n-diffusion inputs are used in GDI as inputs, and output diffusion states are used as outputs. The input signal levels and transistor sizes can be changed to enable the table to perform desired logic operations with less power and time. The GDI function **Table:1** is a vital tool that GDI circuit designers can use to check, assess, and improve their designs for specific applications.

Table 1: Different logic function realization using GDI cell.

N	P	G	Output	Function

0	B	A	A'B	F1
B	1	A	A'+B	F2
1	B	A	A+B	OR
B	0	A	A.B	AND
C	B	A	A'B+AC	MUX
0	1	A	A'	NOT
B'	B	A	A'B+AB'	XOR
B	B'	A	AB+A'B'	XNOR

Table 2 lists how many transistors are needed to implement each function using CMOS logic and the GDI approach.

Table 2: Comparison of Transistors.

Function	CMOS(no. of transistors)	GDI(no. of transistors)
F1	6	2
F2	6	2
OR	6	2
AND	6	2
NOT	2	2
MUX	12	2
XOR	16	4

3. USE OF GDI CELLS IN LOGIC CIRCUIT

GDI cell is used to build various logic circuits such as AND, OR, XOR, XNOR, NAND, NOR, NOT and MUX and DEMUX circuits. These logic blocks are used to build different logic devices which have a capacity of building a more complex logic functions which are further derived based on the necessity. It allows for better optimization of circuit performance, making it possible to achieve more efficient logic functions. It is expected to gain more popularity in the semiconductor industry as power consumption and area become increasingly important considerations in integrated circuit design. These can be used in memory cells which requires fast computational power such as gaming, research purpose etc. The logic gates are as follows:

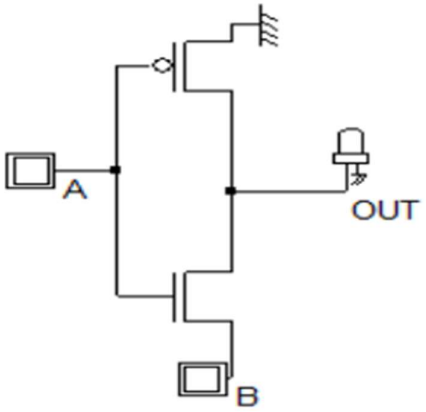

Figure 2: AND gate using GDI cell.

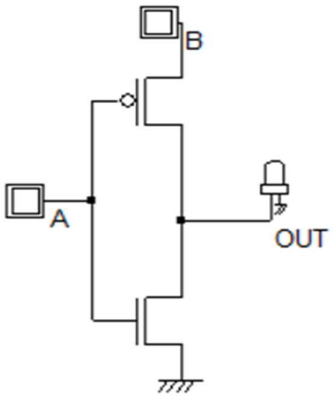

Figure 3: OR gate using GDI cell.

Output=A.B

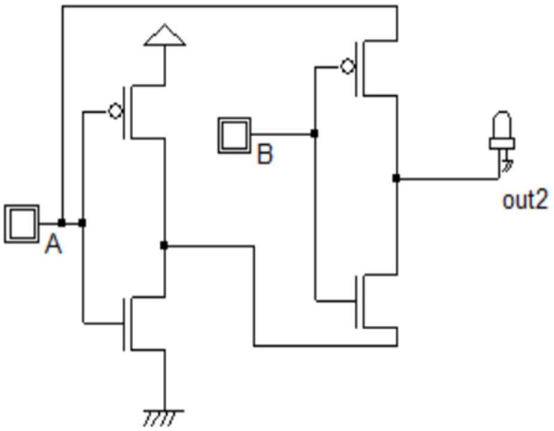

Figure 4: XOR gate using GDI cell.
Output=AB'+A'B

Output=A+B

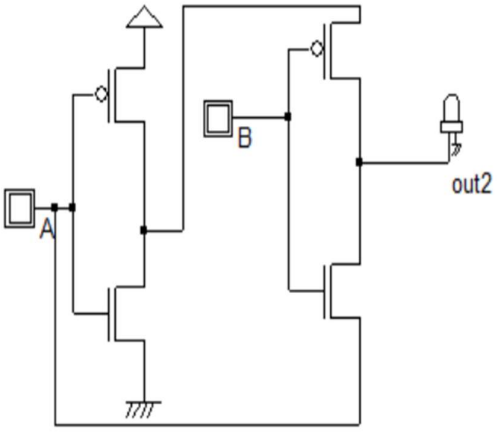

Figure 5: XNOR gate using GDI cell.
Output=AB+A'B'

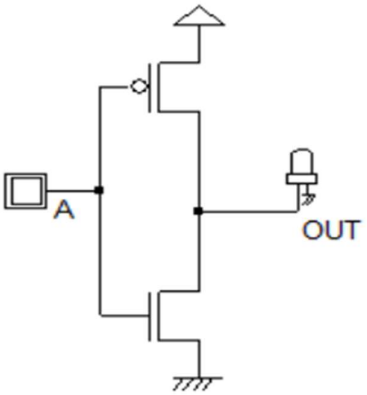

Figure 5.1 : NOT gate
Output=A'

4. FULL ADDER DESIGN

There are various full adders which can be designed using XOR.The number of transistors decreased to get low power consumption. The logic functions used in full adder can be given by these equations.

SUM=A XOR B XOR C.

Cout = (A XOR B) C + AB.

The essential gates required for creating a full adder are AND, OR, XOR, and XNOR, as shown by the above mentioned formulae.

Two transistors and one inverter can be used to create the basic gates, as indicated in the diagram above. **Table 3** displays the whole adder's truth table. Every input is verified by the circuit.

Table 3: Truth Table of full adder

A	B	C	SUM	CARRY
0	0	0	0	0

0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

5. VARIOUS FULL ADDER DESIGNS

5.1.1 14T Hybrid Full adder

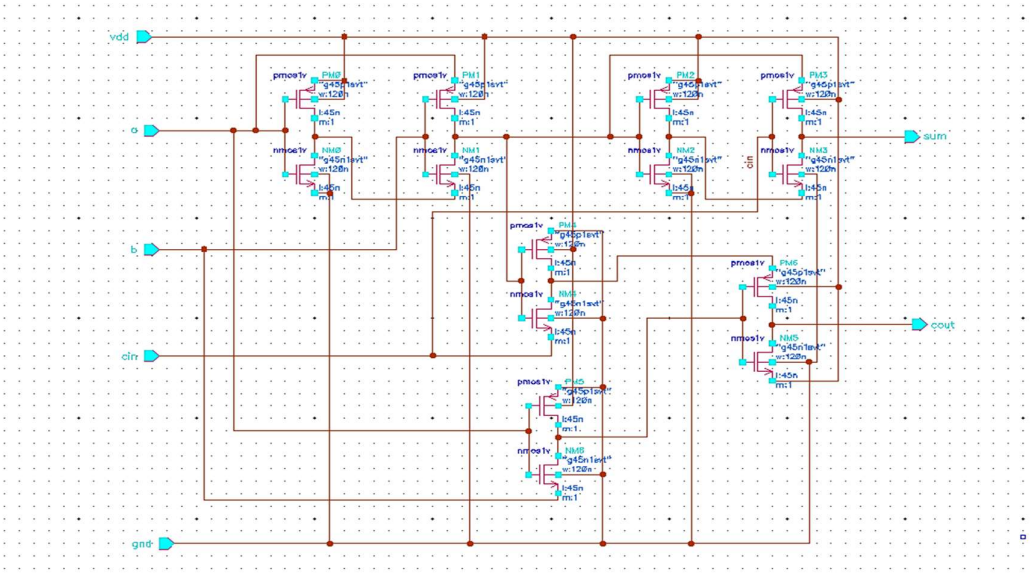

Figure 6 : 14T MVT-GDI hybrid full adder

Only 14 transistors are used in the suggested full adder design, as depicted in Fig. 6. Five logic blocks that were created using the MVT-GDI technique make up most of it. Two multiplexers, one Swing Restored Transmission Gate (SRTG), one Swing Restored Pass Transistor (SRPT) block, one XOR/XNOR, and two multiplexers round out the circuit. The GDI approach is used in the creation of the XOR/XNOR block.

The inverters used in the XOR/XNOR blocks are integrated with typical VT devices since the path of the inverters has no voltage loss. In order to achieve the sum function, the GDI MUX-1 multiplexes the output of the XOR (A XOR B) and the XNOR (A XNOR B) with a control input (Cin).

5.1.2 12T Hybrid Full Adder

The full adder cell has the 12 transistors that is shown in figure 7. In case of this cell, the GDI technique is used for generatingof XOR functions. This stage shows full swing with low voltage. The output of XOR, together with other inputs, will be fed to the other circuit which has to design based on Gate-Diffusion Input (GDI) technique. The Sum and Carry outputs are generated from the final stage.

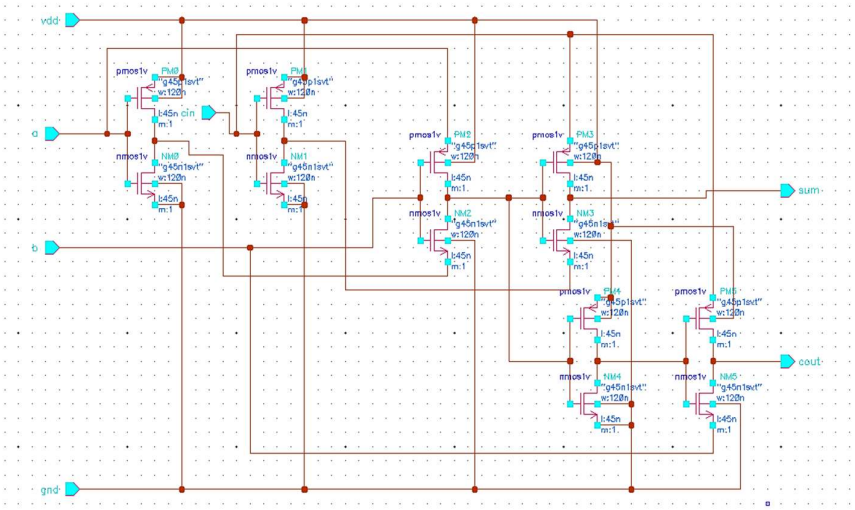

Figure 7 : 12T GDI hybrid full adder

5.1.3 10T Hybrid Full Adder

10T GDI full adder uses 10 transistors to perform the arithmetic addition operation. The full adder use XOR gates, with four transistors, and MUX gates, with two transistors. The XOR cells cascade, with a MUX for the carry. The output of the first cell goes to the second cell which is also a XOR and later it is cascaded to MUX. The second cell's output is SUM, while the MUX's output is the carry. It produces output by adding 3-bits and produces output of 2 bits. One of the outputs is SUM and the other output is Cout. The 10T full adder that uses XOR is shown in Figure 8.

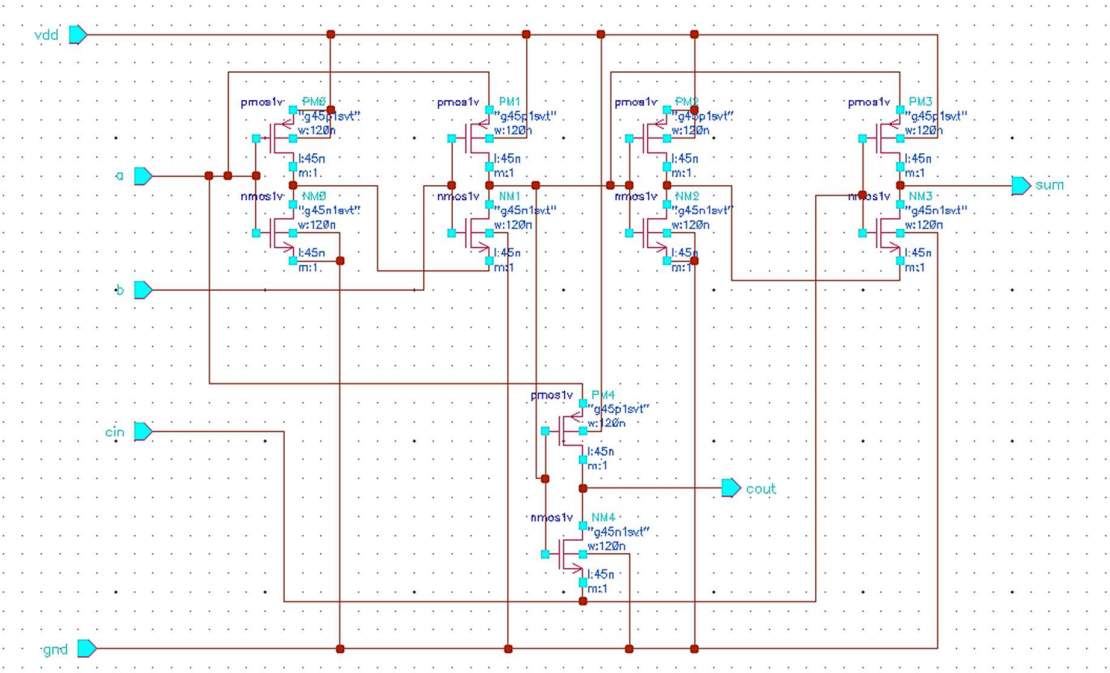

Figure 8 : 10T GDI hybrid full adder

5.1.4 9T Hybrid Full Adder

The 9T full adder employs only 9 transistors, lowering power usage. The first XOR cell uses just 3 MOSFETS - 2 PMOS and 1 NMOS, while the second cell has 4 MOSFETS. The design preserves all required functionality for addition operations, and the suggested circuit is depicted in the figure. This approach provides a practical and efficient way to construct a full adder with minimal power usage.

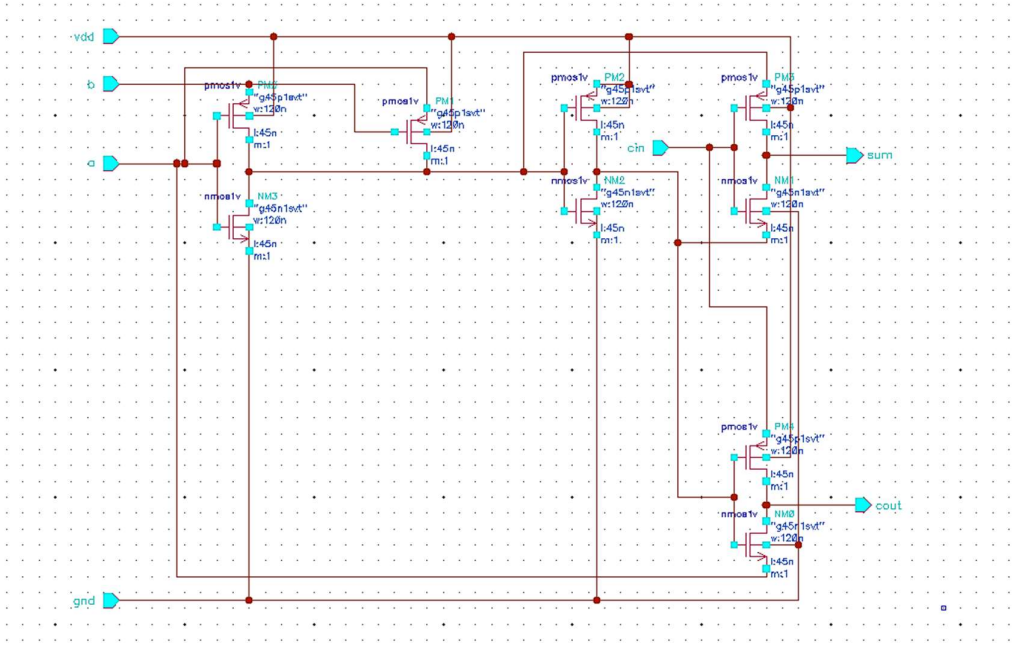

Figure 9 : 9T GDI hybrid full adder

5.1.5 8T Hybrid Full Adder

The 8T MGDI full adder uses 8 transistors with a modified technique, generating SUM and CARRY. It is more power-efficient and has fewer transistors than the 10T gate diffusion full adder, the 16T hybrid full adder, and the CMOS full adder. The design is best suited for low power applications and offers high speed. The full adder has three inputs (A, B, and C) and two outputs (SUM and Cout).

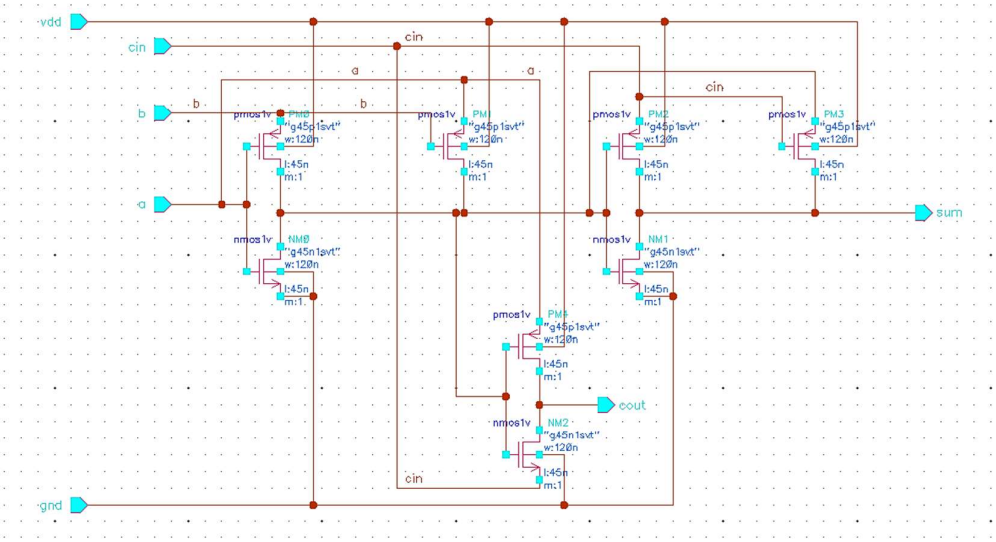

Figure 10 : 8T GDI hybrid full adder

6. SIMULATION RESULT

The simulation of different gate diffusion input full adder is as appeared in the figure below. This waveform gives the best results. Average power and delay are calculated by using this waveform only. Transistors count also considered with the help of waveform.

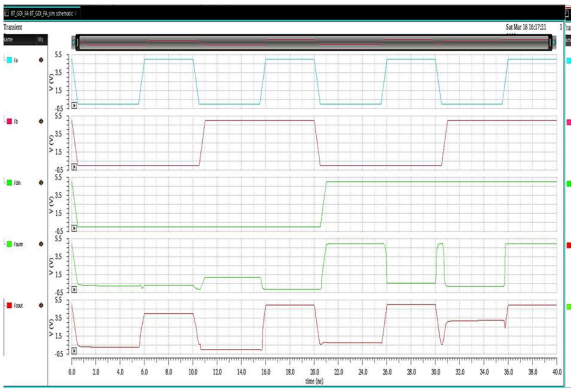

Figure 11 : Simulation results of 8T Hybrid Full Adder

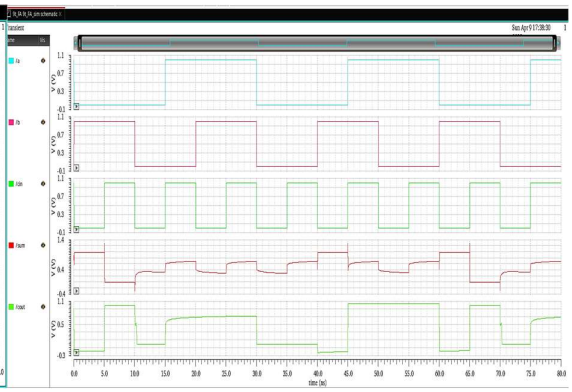

Figure 12: Simulation results of 9T Hybrid Full Adder

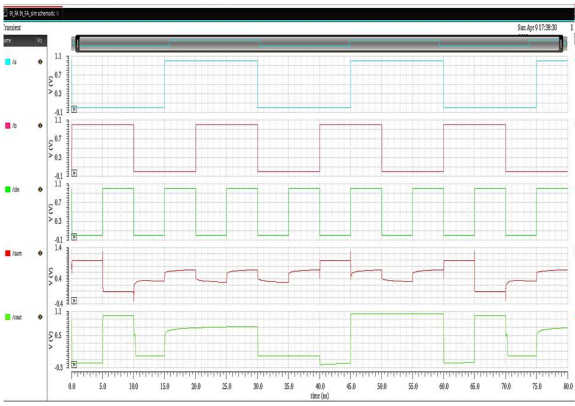

Figure 13 : Simulation results of 10T Hybrid Full Adder

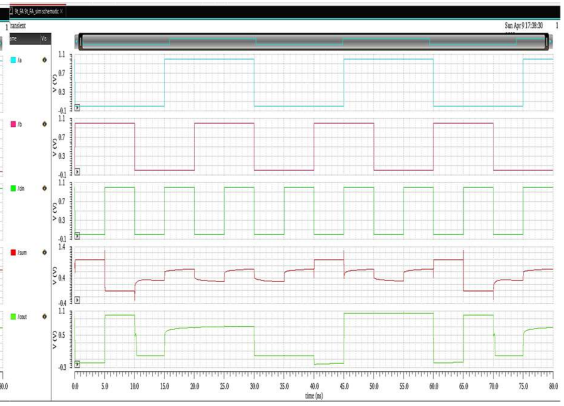

Figure 14 : Simulation results of 12T Hybrid Full Adder

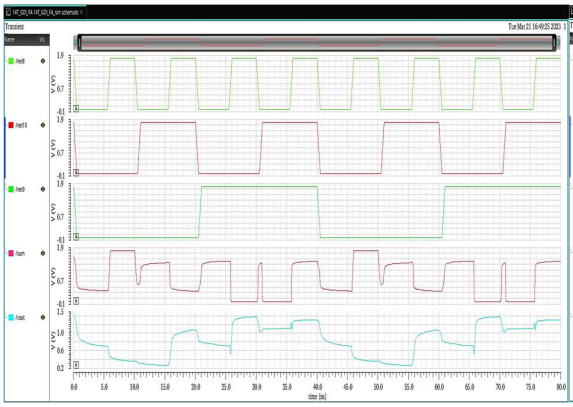

Figure 15 : Simulation results of 14T Hybrid Full Adder

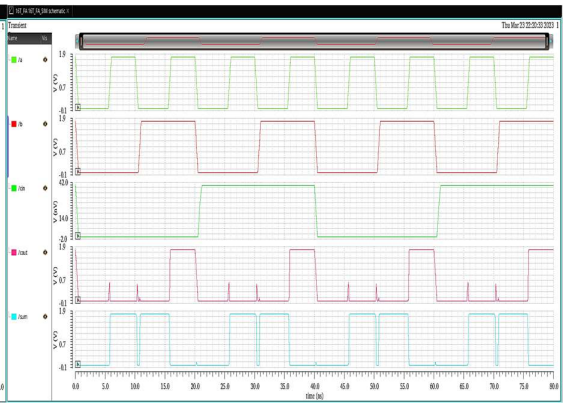

Figure 16 : Simulation results of 20T CPL Hybrid Full Adder

Comparison:

Table 4: Result analysis

S.No	Design	Transistor count	Delay(α)-ns	Average Power(watts)	PDP
1	Conventional full adder	28	2.03e^-3	448.3e^-12	910.049e^-15
2	20T-CPL	20	4.643e^-12	1.556e^-3	7.224e^-15
3	14T	14	5.01e^-9	257.4e^-6	1289e^-15
4	12T	12	3.529e^-12	775.3e^-6	2736e^-18
5	10T	10	35.8e^-12	516.6e^-6	18494e^-18
6	9T	9	5.008e^-9	514.6e^-6	2577e^-15
7	Proposed work(8T)	8	24.9e^-9	83.2e^-12	2071e^-21

CONCLUSION

In this research, a method for creating a GDI cell-based low power full adder is proposed. Less transistors and in cell swing restoration under operating conditions are two benefits of the Gate Diffusion technology. The GDI cell also enables the use of two transistors to accomplish various logic operations. This one-bit complete adder is created by employing variously configured GDI cells. Due to a smaller number of transistor count, the low power is used Here we can see that the conventional full adder has low average power whereas its delay is high making it impossible to use for better and high-performance applications. Certain other Hybrid Adders consists of different delay and average power making it differentiable for the use based on the requirement such as power, delay, area as such. From the above comparison both 12T and 10T can perform arithmetic operations at a higher efficient rate. The simulation is done by using cadence tool. The 8T modified gate diffusion full adder outperforms the 12T GDI full adder, the 10T gate diffusion full adder, and the 9T hybrid full adder in terms of metrics like average power and transistor count. Therefore, it is ideally suited for low power applications and the better 8T modified gate diffusion input full adder.

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