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FIR FILTER DESIGN USING HYBRID REVERSE CARRY PROPAGATE ADDER

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Abstract—Numerous applications of Finite Impulse Response (FIR) Filter have been found in many signal processing applications, biomedical applications, de-noising, etc., It is essential to design the FIR filter with high speed and low power consumption. In this proposed work, design of FIR filter has been made with RCPA. In this paper a reverse carry propagate adder (RCPA) is presented. In the RCPA structure, the carry signal propagates in a counter-flow manner from the most significant bit to the least significant bit; hence, the carry input signal has higher significance than the output carry. This method of carry propagation leads to higher stability in the presence of delay variations. Three implementations of the reverse carry propagate full-adder (RCPFA) cell with different delay, power, energy, and accuracy levels are introduced. The best one is selected and implemented in FIR filter. The proposed structure may be combined with an exact carry adder to form hybrid adders with tunable levels of accuracy. This Proposed RCPFA System Implemented using Verilog and Simulated by ModelSim 6.4a and Synthesized by Xilinx ISE 9.1i tool.

Index Terms - AOI- AND OR Invert, OAI – OR AND Invert , LUT – Look Up Table, RTL – Register Transistor Logic, DCT – Discrete Cosine Transform, DWT – Discrete Wave Transform

I INTRODUCTION

Continuous power consumption reduction and speed improvement are the key goals in the design of digital processing units, especially the portable systems. Normally, an increase in the speed is achieved at the cost of more power consumption for exact processing units. One of the approaches to improve both the power and speed is to sacrifice the computation exactness. This approach, which is approximate computing, may be used for the applications where some errors may be tolerated.

Impulse response in finite period of time is defined as Finite Impulse Response Filter. The majority of its applications are found in the field of signal processing, image processing, speech processing, bio medical signal processing and so on. The outperform characteristics of FIR filter makes it useful for constructing efficient stable filters and those characteristics are linear phase and unconditional stability, ease of implementation, non-existence of overflow

oscillations, greater computational efficiency and the capability to implement filters with co efficient less than one FIR filters can be either continuous in time or discrete in time. The FIR filter can be implemented in software and its design method is based on the approximation of Ideal filter. Windowing techniques are the

basic methods to design these filters. The major purpose of FIR filter is to clip off the unwanted noise and distortion to retains the useful signals. The key factors such as pre-processing, anti-aliasing, band selection, interpolation and low pass filtering makes the FIR filter useful for major signal processing applications. In order to make a filter with no noise as there is no need of truncation or rounding of the bits, FIR filter will become the best option for choosing. A good solution for the practical applications of image processing would be FIR filter.

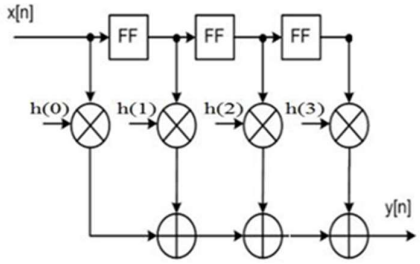

Fig 1. FIR filter

In this paper, we focus on the hybrid adders where the use of the approximate reverse carry propagate full-adder (RCPFA) is suggested. The approximate adder propagates the input carry in a counter-flow manner, i.e., from the higher significant bit to lower significant bit to form the carry output. In this type of adder, which is called reverse carry propagate adder (RCPA), the propagation is performed by introducing a forecast signal acting as an output signal. Owing to the reverse propagation, the weight of the carry decreases as it propagates. This type of adder improves the delay and energy compared to those of the state-of-the-art approximate adders. Also, this adder type is less vulnerable to the delay variation when compared to the conventional ones.

The rest of this paper is organized as follows. In Section II, some related works are briefly reviewed. Different realizations of the proposed RCPFA are described in Section III. The accuracy of the proposed adder is compared to those of the state-of-the-art approximate FAs in Section IV. Section V deals with investigating the design parameters of the suggested FAs and the effectiveness of their use in an error resilient application. Finally, this paper is concluded in Section VI.

II Related works

The same fir filters are implemented by using ripple carry adder. But it has some of the disadvantages over delay and power consumption. Generally ripple carry adder which is a full adder, which takes three binary inputs (two numbers to be added and a carry-in bit) and produces two outputs (the sum of the two numbers and a carry-out bit). The full adder can be cascaded together to form a larger ripple carry adder that can add multiple binary numbers of the same length.The main advantage of the ripple carry adder is its simplicity and ease of implementation using basic logic gates. However, it suffers from a drawback of slow operation

speed since the carry bit must propagate through each stage, which can limit its use in high-speed applications.

For example, consider a 4-bit ripple carry adder that adds two 4-bit binary numbers. The first full adder calculates the sum and carry-out bits for the least significant bits (LSBs) of the two numbers. The carry-out bit from the first full adder is then used as the carry-in bit for the second full adder, which calculates the sum and carry-out bits for the next least significant bits. This process continues through all four full adders until the final sum and carry-out bits are produced.

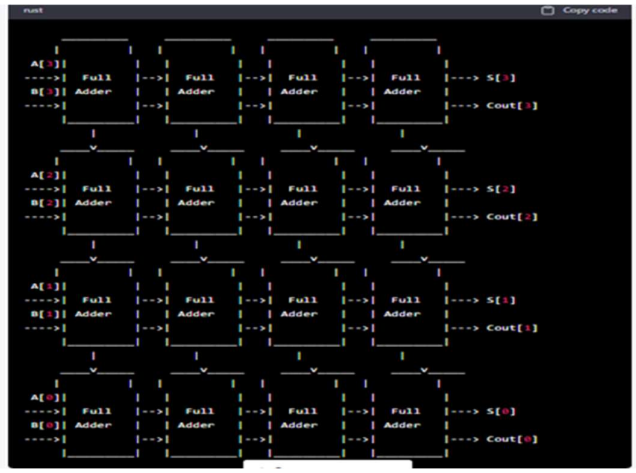

Fig 2. 4 bit RCA

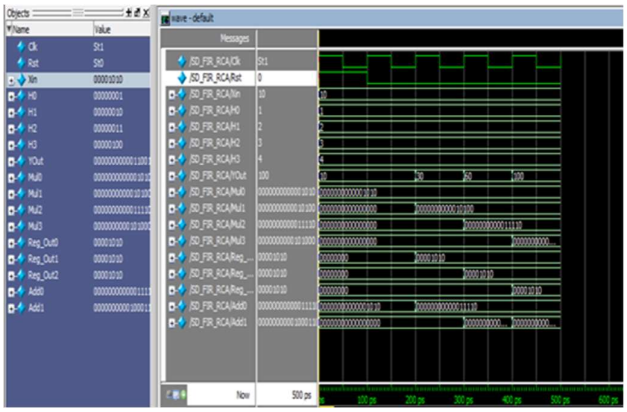

Fig 3. Simulation result of FIR in RCA

The figure 3 shows the simulation result of the FIR filter implementation using ripple carry adder with different inputs. Here Xin is set as 10, booth multiplier multiplication of H0,H1,H2 and H3 respectively 1,2,3,4. And the output of FIR filter Yout is 100.

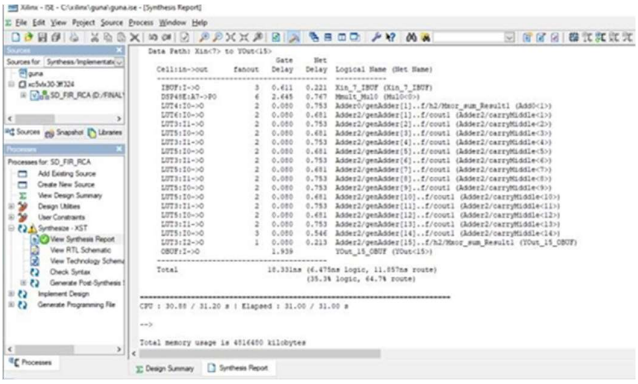

Fig 4. Delay of FIR in RCA

The figure 4 shows the delay of the FIR filter implementation using ripple carry adder. We got total gate delay is about 18.331ns.

Fig 5. Area of FIR in RCA

The figure 5 shows area of FIR filter implementation using ripple carry adder and number of slice LUTs are 71.

When compared these results with our proposed system it has Large power consumption ,Critical path delay has not been reduced.

III Proposed system

To overcome the drawbacks of existing system, We focus on the hybrid adders where the use of the approximate reverse carry propagate full-adder (RCPFA) is suggested. The approximate adder propagates the input carry in a counter-flow manner, i.e., from the higher significant bit to lower significant bit to form the carry output. In this type of adder, which is called reverse carry propagate adder (RCPA), the propagation is performed by introducing a forecast signal acting as an output signal. Owing to the reverse propagation, the weight of the carry decreases as it propagates. This type of adder improves the delay and energy compared to those of the state-of-the-art approximate adders. Also, this adder type is less vulnerable to the delay variation when compared to the conventional ones.

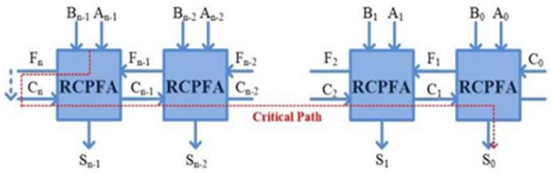

Fig 5. Block diagram of n-bit RCPFA

The Proposed Adder is used to make a Design of FIR. We evaluated the proposed approach by comparison with ripple carry adder. the results based on a rough theoretical analysis and on logic synthesis showed its efficiency in terms of area, delay and power. Simulation results show that the proposed Adder based designs significantly improve the area, delay and power consumption when the word length of each operand in the Adder. So that we have implemented three different hybrid rcpfa adder and after synthesis the best one is selected and

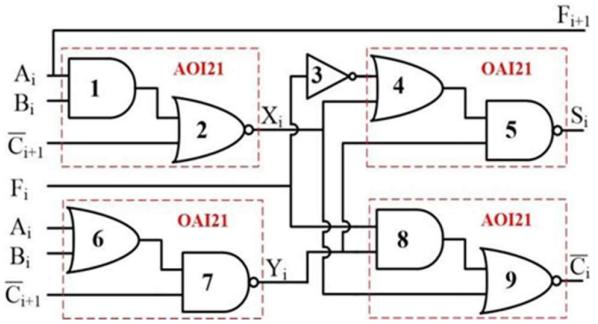

Fig 6. RCPFA-I

Item	A_i	B_i	C_{i+1}	F_i	S_i	C_i	F_{i+1}	X_i	Y_i
1	0	0	0	0	0	0	0	0	1
2	0	0	0	1	1	1	0	0	1
3	0	0	1	×	0	1	0	1	1
4	0	1	0	×	1	0	0	0	0
5	0	1	1	×	0	1	0	1	1
6	1	0	0	×	1	0	1	0	0
7	1	0	1	×	0	1	1	1	1
8	1	1	0	×	1	0	1	0	0
9	1	1	1	0	0	0	1	0	1
10	1	1	1	1	1	1	1	0	1

Fig 7. RCPFA -I truth table

implemented in FIR filter. Finally these RCPFA is Hybrid with full adders.

RCPFA-I:

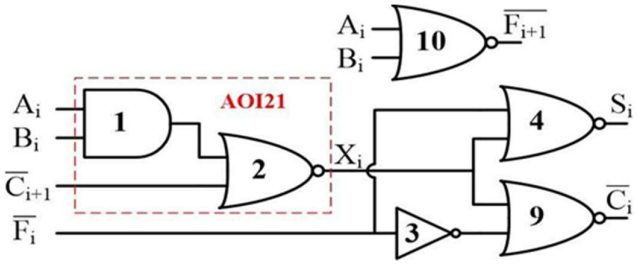

Fig 8 RCPFA-III

Item	A_i	B_i	C_{i+1}	F_i	S_i	C_i	F_{i+1}
1	0	0	0	0	0	0	0
2	0	0	0	1	1	1	0
3	0	0	1	×	0	1	0
4	0	1	0	0	0	0	1
5	0	1	0	1	1	1	1
6	0	1	1	×	0	1	1
7	1	0	0	0	0	0	1
8	1	0	0	1	1	1	1
9	1	0	1	×	0	1	1
10	1	1	×	0	0	0	1
11	1	1	×	1	1	1	1

Fig 9 truth table of RCPFA-III

The proposed RCPFAs may be used in hybrid adders whose general n-bit structure based on the RCPFAs is depicted in Fig. 9 Obviously, the design parameters of the adder depend on the width of the approximate part. using RCPFA-III leads to the smallest delay due to the small less LUTS. RCPFA-III provides the smallest delay. In the cases of the power, energy, for all the approximate part widths, utilizing RCPFA-III (RCPFA-I) results in the smallest.

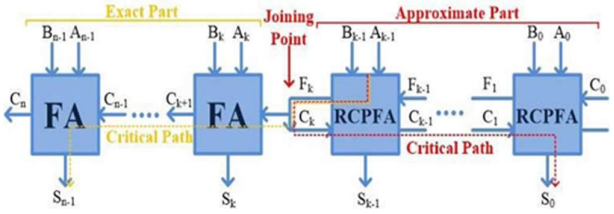

Fig 10 n-bit hyrid RCPFA

HYBRID RCPFA -I

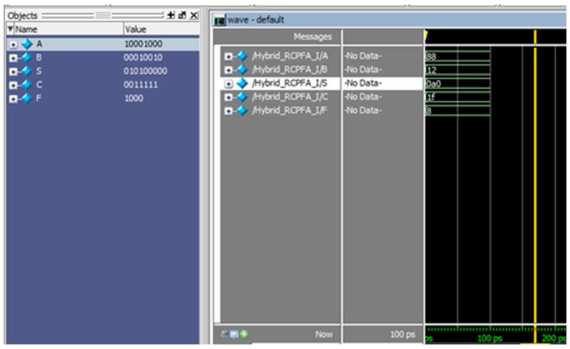

Fig 11 Simulation result of Hyrid rcpfa-I

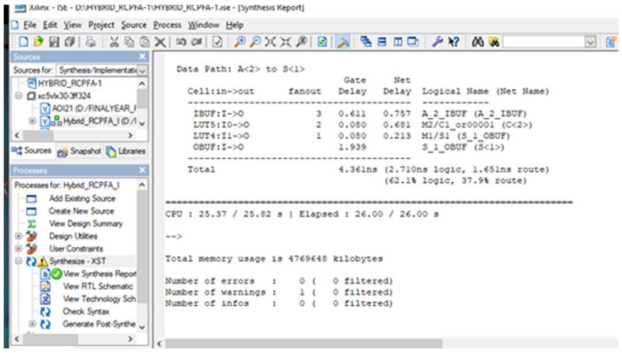

Fig 12 Synthesis of hybrid rcpfa-I The figure 12 shows delay about 4.361ns.

HYBRID RCPFA-II

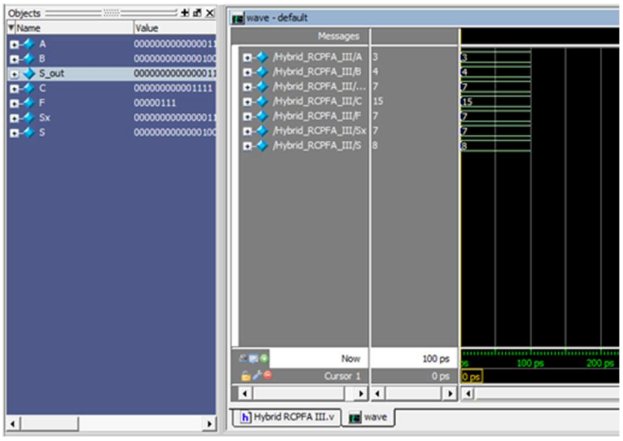

Fig 13 Simlation result of hybrid rcpfa-III

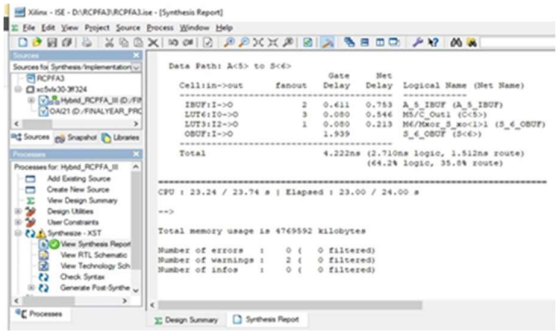

Fig 14 Synthesis of hybrid rcpfa-III

So in figure 14 the gate delay in RCPFA-III is 4.222ns . and this is efficient than other two hybrid adders. So the Proposed FIR filter is designed using hybrid RCPFA-III.

III FIR filter design

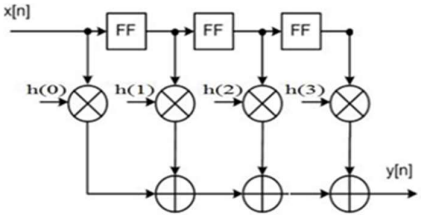

Fig 15 proposed fir filter block diagram

A filters is an instrument or mechanism that eliminates an undesirable part or function from a signal. Filtering is a signal processing class, which indicates that certain parts of the signal are fully or partly removed. Two major filter forms are available, analogue and digital. Depending on the classification criterion, filters can be categorised in many categories. The two main forms of optical filters are digital filters for finite pulse response (FIR) and digital filtering (IIR).

$$out(n) = \sum_{i=0}^{N-1} x(n-i)\,h(i)$$

Finite impulses (FIR) automated filters, for example voice processings, high-level speech equalization, echo cancellation, adaptive noise cancellation, and other connectivity technologies, including software-specified radio (SDR), are commonly utilized in various digital signal processing applications. In order to satisfy the high frequency criteria, many these applications need FIR filters of broad order. These filters also need to help large digital contact sampling speeds. However, for each filter production, the number of multiplications and additions is increased according to the filter order. As the FIR filter algorithm has no redundant computation, real-time implementation in a resource limited setting of a broad order FIR filters is a challenge. Most frequently the filters coefficients stay stable and established applications for apian signal processing. In optical signal processing, FIR filters are generally used.

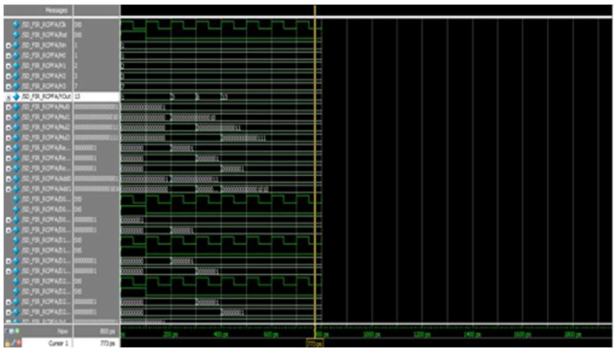

Fig 20 simulation result of FIR filter

In figure 20 the clock and reset are set . After inputs values of Xin, H0, H1, H2, H3 are taken respectively 1,1,2,3,7 and we got Yout as 13. The result is verified successfully.

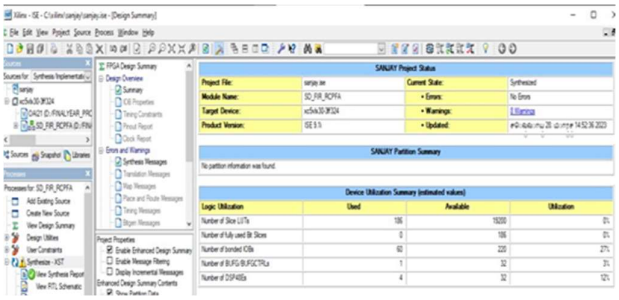

Fig 21 Synthesis result of proposed FIR filter

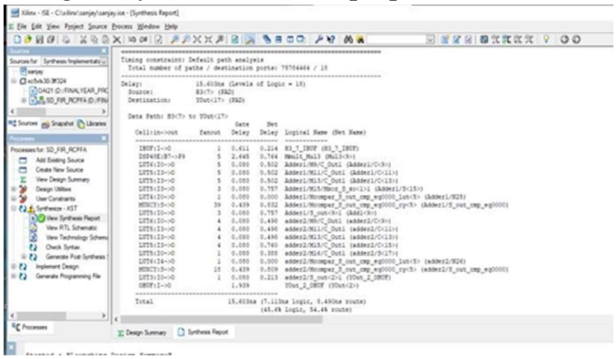

Fig 22 Total gate delay of proposed FIR filter

In figure 22 the total gate delay obtained is 15.603ns. this is less than the existing system.

IV Results and conclusion Table1 Comparison table

S. No	Parameters	Existing system	Proposed system
1.	Delay	18.331ns	15.603ns
2.	Memory	48,23,580Kb	48,16,480Kb
3.	Area	71 LUTs	186 LUTs

IV Conclusion

In this paper, we proposed approximate RCPFAs which propagate carry from most significant to LSBs. The reverse carry propagation provided higher stability in delay variation. The efficacy of the proposed approximate FAs and the hybrid adders which realized them has been studied. Fir filter is implement using reverse carry propagate adder (RCPA).

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