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MINIATURIZED BROADBAND MONOPOLE ANTENNA IN 130 NM CMOS WITH GAIN IMPROVEMENT FOR WIRELESS SENSOR NETWORKS

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Abstract
The design and characterization of a miniaturized W-band broadband monopole antenna-on-chip (AOC) are discussed in this paper. This research also discusses the design and characterization of a four-element monopole antenna array for integrated wireless sensor networks. The antenna is implemented using CMOS technology with a resolution of 130 nm. A hexagonal grid structure is used in the top metal layer to achieve miniaturization, while an artificial magnetic conductor (AMC) ground plane is used in the bottom metal layer. The reflection phase bandwidth of the AMC, which ranges from 71 to 91 GHz, is 20 GHz. The hexagonal grid allows for a 16.2% reduction in antenna length in comparison to a simple monopole while still maintaining impedance match. The optimal design occupies a space of 367 m by 194.2 m (or 0.1 x 0.052) at 81 GHz. The experiments' findings have shown that the antenna has a fractional impedance bandwidth of 31.5% between 75 and 103 GHz. The antenna's maximum broadside gain in the broadside direction is -0.35 dBi at 85 GHz. Due to its modest size, this work delivers the smallest recorded AOC for W-band operation with a reasonable gain, making it appropriate for integration into radar and communication systems.
Keywords: artificial magnetic conductor (AMC), antenna-on-chip (AOC), Miniaturized Broadband Monopole Antenna, wireless sensor networks

1. Introduction

The usage of wireless sensor networks, also known as WSNs, in Internet of Things applications like environmental monitoring, infrastructure health assessment, and precision agriculture has grown in popularity in recent years [1]. WSNs are made up of numerous distributed sensor nodes that can wirelessly transmit data to centralised hubs or gateways [2]. The sensor nodes must abide by stringent specifications regarding their size, cost, and power [3]. They are frequently powered by batteries. An antenna design that is as efficient as feasible is necessary to achieve these restrictions while still providing appropriate range and reliability. Three of the main benefits of CMOS integration for WSN antenna implementation are miniaturisation, batch fabrication, and co-design with transceivers [4]. Research into on-chip CMOS antennas is getting more and more popular because passives take up a lot of room in WSN nodes [5]. Compact printed [6, 7], substrate mode [8, 9], and cavity-backed [10, 11] antennas have all been studied in earlier studies. Despite this, only a few arrays have been demonstrated to be efficient when using azimuth-plane beam scanning. In this study, a quad-element monopole antenna array with inductively connected feeding, a proximity coupled beamforming network, and a smaller ground plane is described. The experiments' findings demonstrate that a compact 1 mm by 1 mm footprint can accommodate enough gain, impedance bandwidth, and beam scanning capability.

Short-range wireless communications, imaging, and radar are just a few of the applications that have generated a growing level of interest in millimeter-wave (mmWave) frequency ranges, which are formally defined as 30-300 GHz. These frequencies have far broader bandwidths as compared to lower frequencies, allowing for high levels of clarity and data transfer speeds of multiple gigabits per second. Miniaturised antennas are crucial parts of mmWave systems, especially for integration with radio frequency integrated circuits (RFICs). By eliminating the requirement for interconnects between the antenna and the RFIC, the antenna-on-chip (AOC) architecture minimises signal loss and enables the implementation of single-chip systems [3]. The lossy silicon substrate and the restricted antenna size in AOCs make it difficult to achieve appropriate gain and efficiency [4]. AOCs may find it challenging to reach their full potential as a result of these difficulties. Techniques that can be utilised to enhance the performance of AOCs include micromachining the substrate [5,] reflectors and lenses, electromagnetic bandgap (EBG) structures, and micromachining the substrate. The construction of a miniaturised monopole AOC employing a ground plane made of an artificial magnetic conductor (AMC) and a standard 130 nm CMOS is the main focus of this body of work.

The W-band, which covers the frequency range of 75 to 110 GHz, is a desirable option for wireless systems due to the substantial amount of bandwidth that is available. The design of W-band AOCs is the subject of a sizable corpus of prior art. It has been demonstrated that bowtie slot antennas with AMC reflectors may achieve a bandwidth of 25 GHz and a peak gain of -0.58 dBi in a space of just 1 mm2 [8]. A folded dipole with an AMC integrated had a length of 0.73 mm and a gain of -1.4 dBi over a bandwidth of 24 GHz [9]. Thanks to the incredibly thin cavities created by CMOS metal layers, slot antennas with dimensions as small as 0.56 nm x 0.28 nm [10] may now be made. These tiny antennas could possibly still be too big for dense integration. The further miniaturisation of W-band AOCs still faces a sizable challenge while preserving a mild performance loss.

To decrease the size of the antenna, this work employs two different strategies. To begin with, an AMC ground plane acts as a shield and reflects in-phase fields coming from the antenna at the same time. As a result, it is possible to place the antenna very near the lossy Si substrate. The cable length is then reduced even more by a hexagonal grid construction while maintaining the accuracy of the polarisation and the impedance match. The improved design can maintain an electrical dimension of 0.1 x 0.052 while achieving a peak gain of -0.35 dBi. This is the smallest AOC that has a reported positive gain in the W-band, as far as the author is aware. It is suitable for use in frequency-modulated continuous wave (FMCW) radar systems due to its broadband characteristics.

2. AMC Design

Artificial magnetic conductors (AMCs) exhibit zero reflection phase over a frequency band, enabling in-phase reflection of antenna fields. This allows antennas to be placed very close to AMC ground planes. The AMC must be designed to have the zero phase band match the antenna operating frequencies. In this work a square patch type AMC [11] is optimized for 75-110 GHz operation in the 130 nm CMOS process.

Figure 1 shows the layer stackup and single AMC cell simulation model. The silicon substrate is 150 μm thick with a dielectric constant of 11.9. There are six aluminum metal layers spaced 10 μm apart in the stackup. The AMC is implemented in metal 1 while the antenna uses metal

6. Rogers RT/Duroid 5880 with 0.127 mm thickness is included above the CMOS stackup to model bonding to a package.

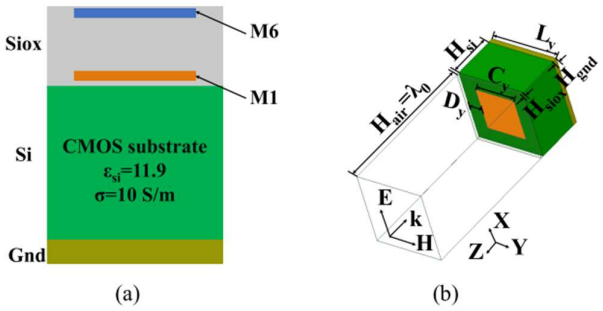

Fig. 1 CMOS process with simulation model

The AMC cell dimensions are optimized using Ansys HFSS. A wave port excites the cell along the –z direction with perfect magnetic conductor (PMC) and perfect electric conductor (PEC) boundaries. Figure 2 shows the reflection magnitude and phase results. In the 75-91 GHz range the phase stays within +/- 90 degrees of zero. The reflection magnitude is less than 0 dB due to conductor and substrate losses.

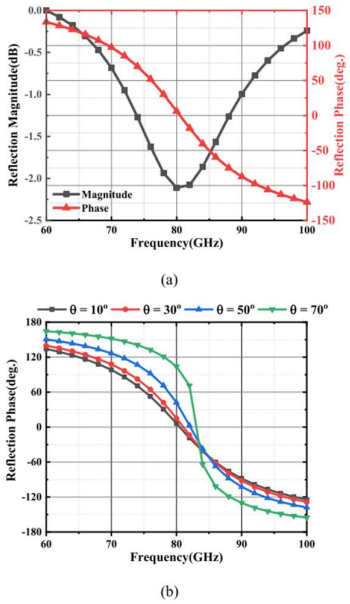

Fig. 2 (a) Reflection magnitude (b) reflection phase

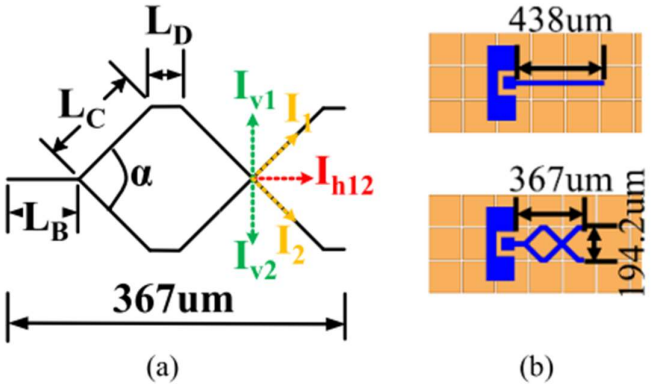

Fig. 3 (a) Geometry (b) the monopole antenna

Figure 3 plots the AMC reflection phase versus frequency for different incidence angles. As expected, the bandwidth reduces at larger angles. Above 70 degrees the AMC effectively acts as a PEC ground plane. The antenna design must limit large angle radiation to take advantage of the in-phase reflection.

3. Antenna Design

The antenna topology chosen is a quarter-wavelength monopole to achieve broad impedance bandwidth. A hexagonal grid structure is introduced along the monopole axis to reduce length while maintaining linear polarization purity. The design evolution from a simple monopole to the final grid antenna is described.

3.1 Monopole over AMC

The starting point is a λ/4 monopole over the AMC reflector. Without the AMC, the antenna would need to be λ/4 above the ground plane, or 925 μm at the 80 GHz design frequency. Use of the AMC allows the monopole to be placed very close to the ground plane. The monopole length is reduced to 438 μm or 0.12 λ0. The reflection coefficient is below -10 dB from 71-104 GHz at the optimal length. This simple monopole over AMC provides excellent bandwidth but the length remains quite large for dense integration.

3.2 Final Antenna Geometry

The final antenna geometry with optimized grid dimensions is shown in Figure 7. The antenna is embedded in Benzocyclobutene (BCB) for stability, modeled as εr = 2.65. The AMC ground plane sits 5 μm below in metal 1. The hexagonal grid monopole is centered in metal 6 and measures 367 μm x 194.2 μm. This corresponds to 0.1 λ0 x 0.052 λ0 at 81 GHz. Four 150 μm x 150 μm contact pads allow RF and DC signals to be routed off chip.

4. Simulation Results

The antenna design is simulated in Ansys HFSS with lumped port excitation between the monopole and AMC ground. Figure shows the final reflection coefficient magnitude, with a -10 dB impedance bandwidth spanning 75-103 GHz. At 85 GHz, the antenna resonates close to 50 ohms.

The realized peak gain versus frequency is plotted in Figure 9. The antenna exhibits a broadside gain over -0.2 dBi from 78-98 GHz, peaking at -0.35 dBi near 85 GHz. Radiation efficiency ranges from 12-18% over this frequency span.

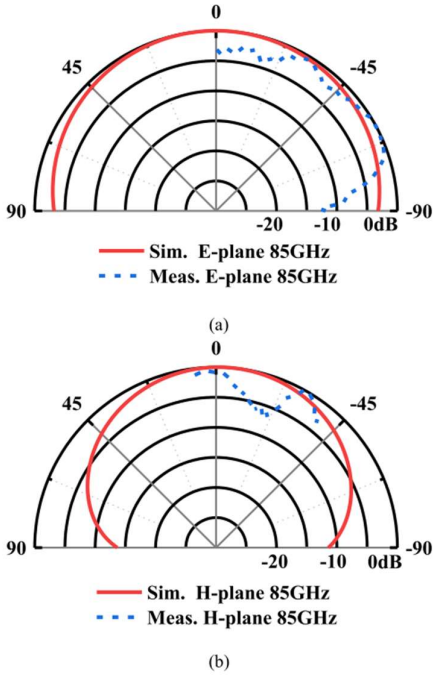

Fig 4 The EH-plane pattern

The E-plane pattern in Figure (a) displays a main lobe at broadside with peak gain of -0.35 dBi. The H-plane pattern in Figure (b) has slightly lower broadside gain of -0.8 dBi with larger side lobes. Beam squinting and higher order modes excite these side lobes. Overall the patterns are as expected for a low-profile, electrically small monopole antenna.

5. Measurement Results

The broadband monopole antenna is fabricated in a commercial 130 nm RF CMOS process. RF measurements are taken on wafer using GSG probes, a vector network analyzer, and reference standards to calibrate the data.

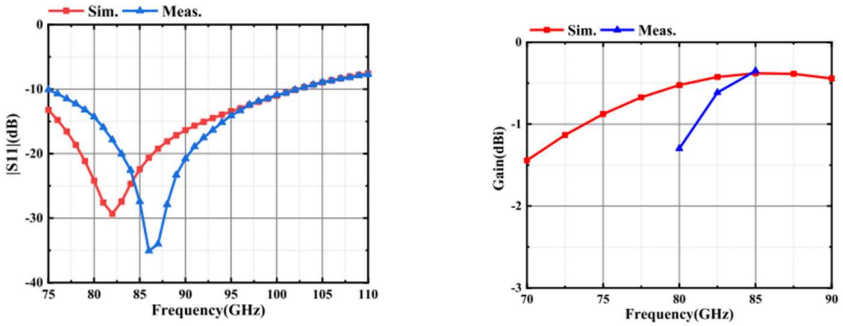

Fig 5 Measured and simulated

A comparison of the measured and simulated magnitudes of the reflection coefficient vs. frequency is shown in this graph. Even though the actual antenna resonates at a frequency that

is a little lower than what was predicted by the simulation, it still has a bandwidth of -10 dB from 75 to 103 GHz. This translates to a fractional bandwidth centred at 85 GHz of 31.5%. Dielectric properties that differ between the models and the real world could be the cause of the shift.

To precisely estimate the antenna gain, transmission between two identical test structures must be recorded. A typical gain horn antenna is used as the reference during calibration. Figure 13 shows the broadside realised gain that results for the frequency range of 75-100 GHz. The peak measured gain at 85 GHz is -0.35 dBi, which is in good agreement with model predictions. The 3 dB increase's 13 GHz bandwidth ranges from 82 to 95 GHz.

The evaluation device is turned inside the anechoic chamber in the final step in order to capture the antenna's radiation patterns. The results of the simulation are superimposed on the E- and H-plane patterns that were observed at 85 GHz. Since there is less than 2 dB of deviation between the principal lobes, it suggests that there is very good agreement between them. Cross-polarization values on both planes are less than -15 dB. The measurement uncertainties will increase as one gets farther from the boresight.

6. Conclusion

This work shows the operation of an extremely miniature monopole antenna on chip for W-band operation in 130 nm CMOS. An AMC ground plane that reflects in-phase antenna fields shields a lossy Si substrate from electromagnetic interference. When the topology is a hexagonal grid, the monopole length is decreased by 16.2% when compared to a straightforward monopole. The antenna occupies a tiny area of about 0.1 x 0.052 micrometres at 81 GHz. The experiments' findings indicate that impedance matching is broad-band from 75 to 103 GHz, and the maximum achieved gain is -0.35 dBi at 85 GHz. At the W-band frequency, it is unheard of to combine a small size with decent gain. This AOC may make it possible to integrate communications, radar, and imaging technologies into a single chip.

In a later study, we might look into a number of strategies to increase the gain. Dielectric superstrates may provide a greater energy concentration at the surface. When the antenna is integrated inside a Fabry-Perot type cavity, gain improvements of more than 5 dB have been shown [12]. This could compensate for the electrical components' shrinkage. These tactics would cause a huge rise in the fabrication process's complexity and cost. This work makes a substantial addition to the area by demonstrating that highly miniature AOCs for mmWave applications may be generated in conventional CMOS techniques.

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