Journal of Data Acquisition and Processing
ISSN: 1004-9037
https://sjcjycl.cn/
DOI: 10.5281/zenodo.7765603

EFFECTIVE DESIGN OF COMBINATIONAL HALF-ADDER AND SUBTRACTOR CIRCUITS DESIGN BASED ON NANOELECTRONICS USING QCA TECHNOLOGY

Dilip Kumar Sharma[1], Prachi Goyal[2*], Praveen Kumar Patidar[3], Suyog Munshi[4], Pranav Paranjpe[5] Mangukiya Hiteshkumar Bhupatbhai [6]
Department of Electronics and Communication Engineering [1, 2, 3, 4, 5, 6]
Ujjain Engineering College, Ujjain (Madhya Pradesh), India [1, 2]
Sushila Devi Bansal College of Technology Indore [3]
Prestige Institute of Engineering Management And Research [4]
Indore Institute of Science and Technology, Indore (Madhya Pradesh), India, 453111 [5]
Gangamai College of Engineering, Nagaon, Maharashtra, India [6]
drdilipsharma@uecu.ac.in[1], goyalprachi7009@gmail.com[2], pravinkpatidar@gmail.com[3], smunshi@piemr.edu.in[4], pranav.paranjpe@indoreinstitute.com [5],
hiteshmangukiya181@gmail.com [6]
[*]**Corresponding authors:** Prachi Goyal (goyalprachi7009@gmail.com).

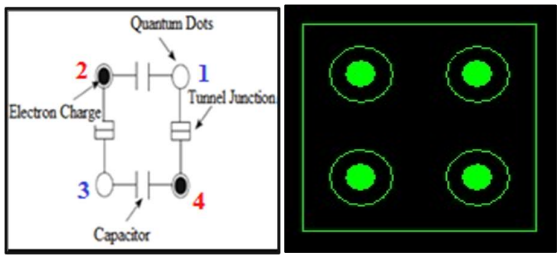
Abstract: Quantum dot Cellular Automata (QCA) is a novel and potentially attractive technology for implementing computing architectures at the Nano-scale. The basic Boolean primitive in QCA is the majority gate. The Quantum Devices for Advanced Nano-electronic Technology project work is the development of a technology for the implementation of different logic circuits based on Quantum Cellular Automata (QCA) architecture. QCA cells characterized by two possible polarization states. The logical structures using QCA has been designed and tested using QCA Designer software. The operation of the structures has been verified according to the truth table. Quantum-dot cellular automata is a novel nanoelectronics nanotechnology that promises very smaller size of digital circuits, very low power consumption, with high speed, minimum delay and operation at Thz (Tera-Hertz) frequencies are highly desired features in the design and fabrication of digital logic circuits. It is considered as a resolution to the scaling problems in CMOS (complementary metal oxide semiconductor) technology. In this paper investigates the quantum-dot cellular automata technology as an alternative to conventional CMOS technology for implementing the nano-scale half adder and half subtractor circuits. The proposed design is proved to be efficient in term of minimum cell count, minimum area in μm^2, low delay from input to output and circuits complexity. The proposed design simulated by using QCADesigner tool V. 2.0.3. The simulated results were verified according to the truth table.

Keyword: Majority Gate, Nanotechnology, Nanoelectronics, Quantum-dot cellular automata, Half-adder, Half-Subtractor.

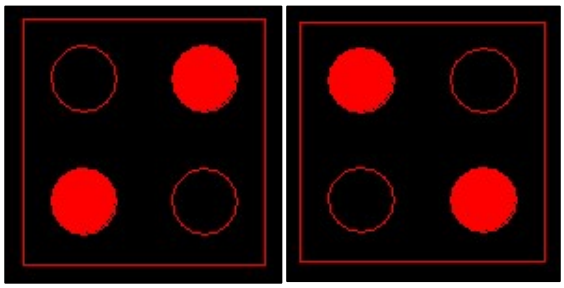
I. INTRODUCTION

QCA (Quantum-dot Cellular Automata) is a promising nanotechnology to create electronic circuits for computing devices and suitable candidate for next generation of computing systems

[1]. It is a way to create digital electronic devices without using transistors that has potential to be faster, denser and more energy efficient than CMOS (complementary metal oxide semiconductor) technology. The fundamental QCA logic primitives are the three input majority gate or Majority Voter (MV) wire and inverter [2].The current CMOS technology is going to approach a scaling limitation in deep nano-meter, nano-technologies [1]. Over several decades QCA has gained a lot of attention as it offers low power, operation at high frequency (THz) and high density for implementing any digital logical circuit [2]. The new transistors less QCA technology was first introduced in 1993[3] from the university of Notre Dame [3, 4] and experimentally verified in 1997. It is a promising nanotechnology to create electronic circuits for computing devices and suitable candidate for next generation of computing systems [4].
The basic elements for QCA logic circuit design are wire, inverter, and 3-input majority gate [4-10]. The QCA wire is formed by an array of quantum cells, the QCA inverter is built by placing quantum cells structure, it is a simple device that inverts an input signal. The majority voter (MV) consists of four QCA cells around a centre QCA cell, of only three input QCA cells and one output cell [5, 6]. The Coulomb interaction between neighboring molecules provides device to device coupling [6] and the physical interactions between quantum cells may be used to realize elementary Boolean logic functions [9]. The Fig. 1 shows the Quantum-dots (90° cells) with polarizations.



1(a): QCA Cell **1(b): Empty cell (P=0)**



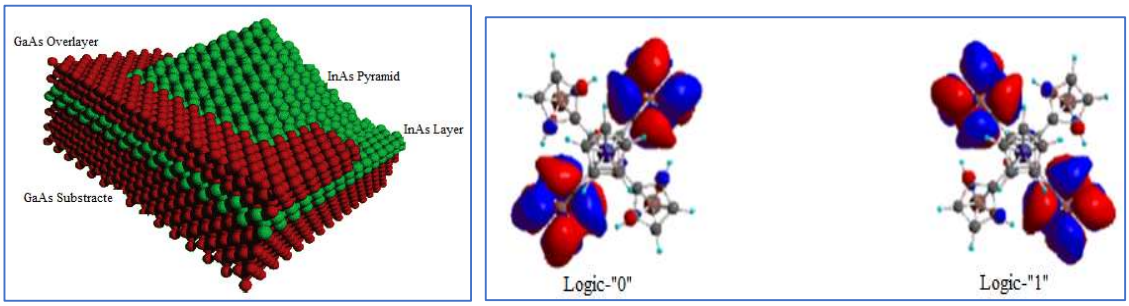
1(c): P = +1(Binary 1) **1(d): P = -1(Binary 0)**

Fig.1: Quantum-dots (90° cells) with polarizations [2, 7]

II. CREATION OF QUANTUM DOT PYRAMID

Quantum dots are nanostructures created from standard semi conductive materials such as InAs/GaAs [5]. These structures can be modeled as 3-dimensional quantum wells. As a result, they exhibit energy quantization effects even at distances several hundred times larger than the material system lattice constant. A quantum dot can indeed be visualized as a well. Electrons, once trapped inside the dot, do not alone possess the energy required to escape. We can use quantum physics to our advantage because the smaller a quantum dot is physically, the higher

the potential energy necessary for an electron to escape. The figure 2(a), below shows an example of a quantum dot given by Konard walus et al (2004). The two possible polarizations of this molecule are shown in Figure 2(b).



(a) **(b)**

Fig. 2 (a): Example quantum dot pyramid created with InAs/GaAs, Fig. 2(b): QCA cell molecule polarizations and the respective logic values.

III. QCA LOGIC LAYOUT DESIGN

QCA logic gate and circuit designers require a rapid, accurate simulation and design layout tool to determine the functionality of QCA circuits in the cell is an elementary building block which can be used to build logic devices and basic gates in QCA architecture.

A. QCA Wire

The simplest arrangement of QCA cells is given by placing them one after another in series forming a QCA wire. If the polarization of the leftmost cell is forced to assume a particular state by applying external electric field, the rest of the cells would immediately synchronize to the same polarization due to electrostatic interactions (Coulombic Law) between them [8]. In a QCA wire, the binary signal propagates from input to output because of the electrostatic interactions between cells. The propagation in a 90° QCA wire [16] is shown in Fig. 3(a) another is (QCA inverter chain) 45° QCA wire, in Fig.3 (b). In an inverter chain, all the cells are 45° rotated from the normal QCA cells. Hence, the final output cans same or the inverted value of the input depending on whether the number of cells between input and output is even or odd.

Fig. 3(a): Layout of "QCA Wire" for 90^0

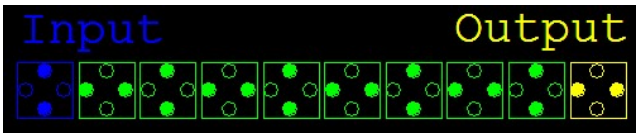


Fig. 3(b): Layout of "QCA inverter chain" for 45^0

B. QCA Inverter

QCA inverter is a simple device that inverts an input signal. The electrostatic interaction is inverted, as the quantum dots corresponding to different polarizations are misaligned between

the cells [2] or QCA is performed by diagonal arrangements of two cells. In this manner input signal is inverted via electrostatic interaction between two diagonally connected cells. This anti-aligning behavior can be used in designing a QCA inverter Fig. 4(a) 2-cell inverter, 4(b) 3-cell inverter configuration and 4(c) QCA Inverter Circuit, shows the basic diagram of a QCA inverter circuit. The "information" is propagating from left to right [11-14].

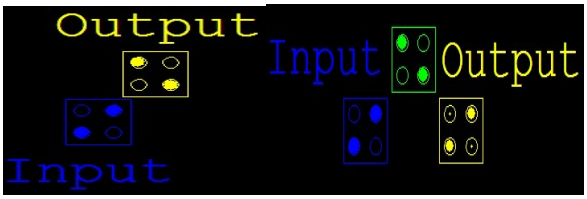


Fig. 4(a): Layout of 2-cell inverter Fig. 4(b): 3-cell inverter

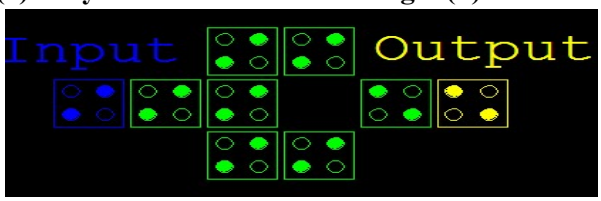


Fig. 4(c): Layout of "QCA Inverter Circuit"

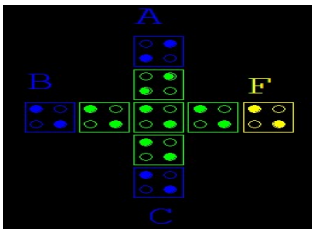
C. QCA Majority Logic

The majority function or majority voter consist of only three input QCA cells [3] implements the logic function is Eq.1. Where A, B, and C are inputs and F is the single output as shown in fig.5 (a).

$$F = AB + BC + AC \qquad (1)$$

It is possible to create a larger majority gate or majority voter which has five inputs. The five-input majority gate works in the same manner as the three input majority gate. If we define the inputs as A, B, C, D, and E, then the equation for its output F can be expressed by the Eq. 2 and shown in fig.5 (b). The five input majority gate can significantly reduce the hardware requirements for complex QCA circuits. Also, it facilitates QCA circuits to be simpler in level, gate counts and clock [11-15].

$M(A,B,C,D,E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE \qquad 2$



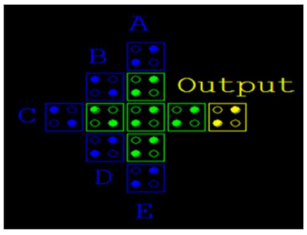


Fig. 5(a): 3- input QCA cells Fig. 5(b): 5- input QCA cells

Fig. 6: Layout of majority voter

D. QCA AND Logic and OR Logic Gate

Majority gate consist of only 3 QCA cells, by fixing a single input to 0, an AND gate can be implemented as shown in Fig. 6(a), whereas fixing an input to 1 implements an OR gate shown in Fig. 6(b). The logic expiration of fixing one of the inputs to the +1 and -1, two input OR Eq. 3 and two input AND gate Eq. 4 is obtained respectively [12-21].

$$AND(A,B) = M(A,B,0) = AB, for\ logic\ AND\ Gate \quad 3$$

$$OR(A,B) = M(A,B,1) = A + B, for\ logic\ OR\ Gate \quad 4$$

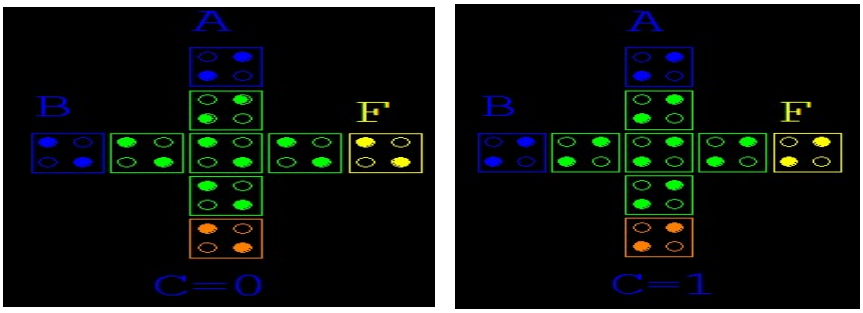


Fig. 6(a): Layout of QCA AND Gate Fig. 6(a): Layout of QCA OR Gate

IV. PROPOSED DESIGN OF ADDER AND SUBTRACTOR CIRCUITS

The quantum-dot cellular automata (QCA) based "nano-communication technology" is a growing field of research at present. But until now very few QCA works are reported of nano-communication, in field of combinational logic circuits (CLC), sequential logic circuits (SLC), memory elements, reversible computing or reversible logic gate (RLG) and networking [16]. The quantum-dot cellular automata are novel developed paradigm nano-technologies and the new alternative of transistor-based technologies [Lent, C. S., et al., 1993 [17], Bahar, A. N., et al., 2018 [18] for its small size, ultra-low power consumptions in different nano-computational functions [19]. In QCA, the basic key-element is the "cell or quantum cell". Which is containing multiple quantum-dots and "interaction-amid cells are purely coulombic and there is no-physical transport of charge".

The half-adder is performs addition of 2 digital bits. There are 2-inputs and 2-outputs in a Half-adder. The inputs are A and B, and the outputs are Sum (S) and Carry (C). The Sum is XOR (Exclusive-OR) of the inputs A and B. Carry is AND of the input A and input B.

Table 1: TT of the half-adder and half-subtractor

INPUTS		**OUTPUTS**			
Input		Half Adder Output		Half Subtractor Output	
A	**B**	Sum (S)	Carry (C)	Difference (Diff.)	Borrow
0	0	0	0	0	0
0	1	0	1	1	1
1	0	1	0	1	0
1	1	1	1	0	0

From the TT (truth-table) of the half-adder, we can see that the SUM (S) output is the result of the Exclusive-OR (XOR) gate and the Carryout (C_{out}) is the result of the AND gate. Then the Boolean expression for a half-adder is as follows equation number 5 and 6.

For the Sum(S) and Carry(C) bit: $SUM = A\ XOR\ B = A \oplus B$ (5)

$$CARRY = A\ AND\ B = A.B \quad (6)$$

Half-subtractor is used to subtract one binary digit from another to give difference output and a borrow output. The truth table of a half-subtractor is shown in table 1. The Boolean expressions for half-subtractor are in equation 7 and 8:

For the Difference and Borrow bit: $Diff. = A\ XOR\ B = A \oplus B$ (7)

$$Borrow = \overline{A}\ AND\ Y = \overline{A}.B \quad (8)$$

IV. SIMULATION RESULTS

To verify our proposed half adder and substractor multilayer layout designs of different logic gates on used recent specific resolution tool QCA Designer version 2.0.3 with the bistable simulation engine setup [16-20]. In this design used the cell size is 14×14 nm^2. The half adder design used 92 quantum cell, cell area0.08 μm^2 and latency 0.75 at shown in figure 7 layout design and other design half substractor 95 cell used, design area 0.07 μm^2 and latency 0.50 at shown in figure 9 layout design. Table 2 contains a comparison between our proposed half adder and substractor design. The cost value was determined by the following Eq. 9. The simulation results of half-add and half-subtractor are shown in Fig. 8 and Fig. 9 respectively.

$$Cost = Area * Latency^2 \quad (9)\ [10]$$

Where area is the size of the design in μm^2 and Latency is the number of clock cycles.

Table 2: Result analysis of proposed half adder and subtractor

Proposed Design	Number of Cells used	Design Area	Latency	Cell size	Cost
Half Adder	92	0.08 μm^2	0.75	14×14 nm^2	0.045
Half Subtractor	95	0.07 μm^2	0.50	14×14 nm^2	0.017

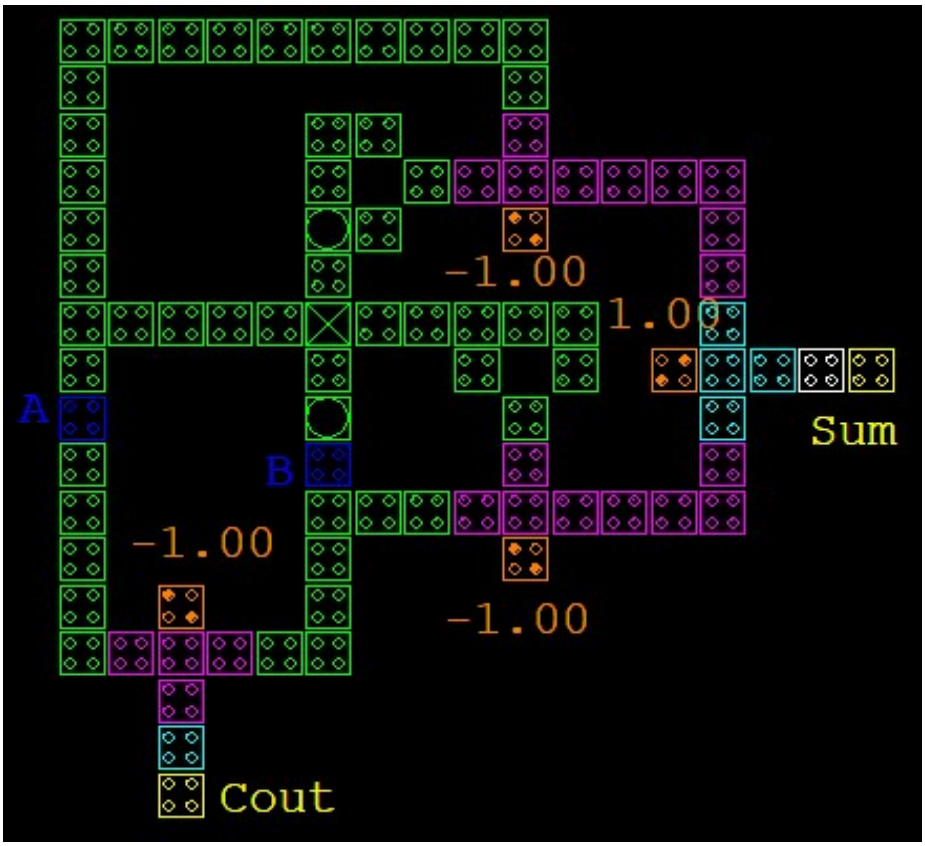


Fig. 7: Multi-layer layout of half-Adder

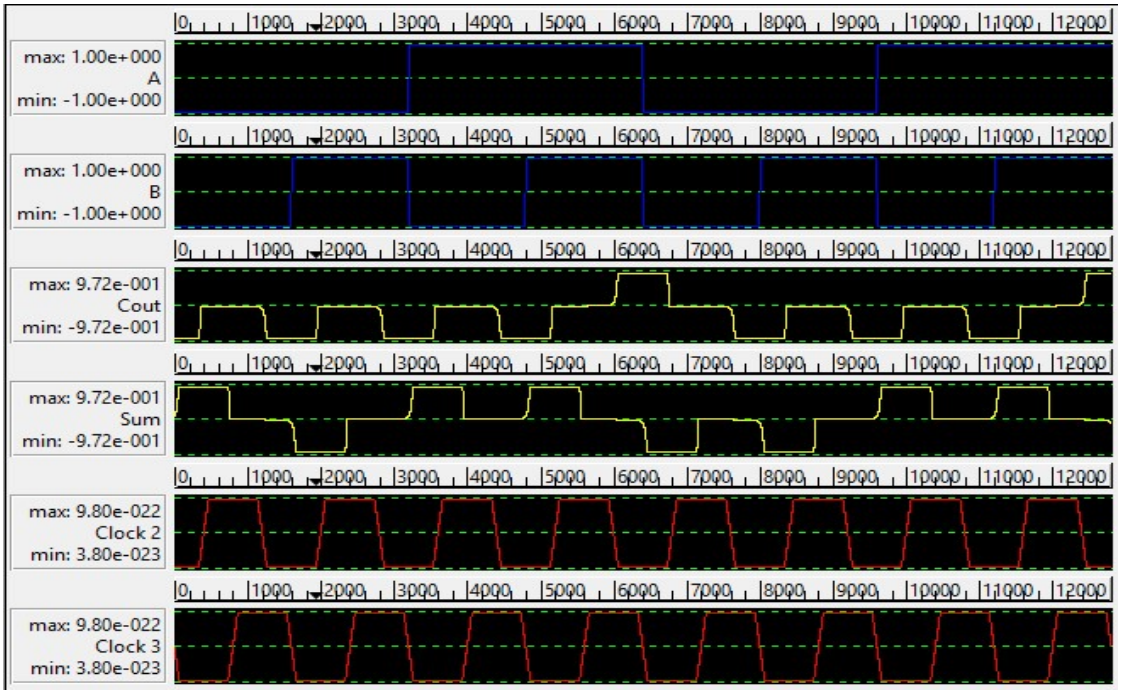


Fig. 8: Simulation results for proposed half adder using 92 quantum cells

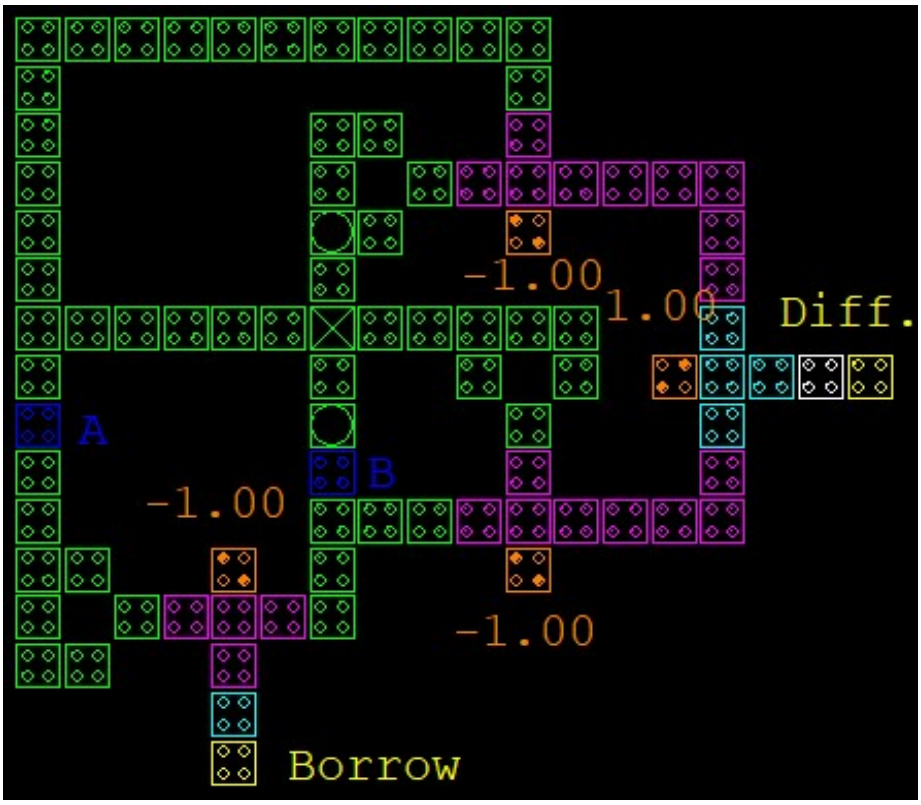


Fig.9: Multi-layer layout of half-subtractor

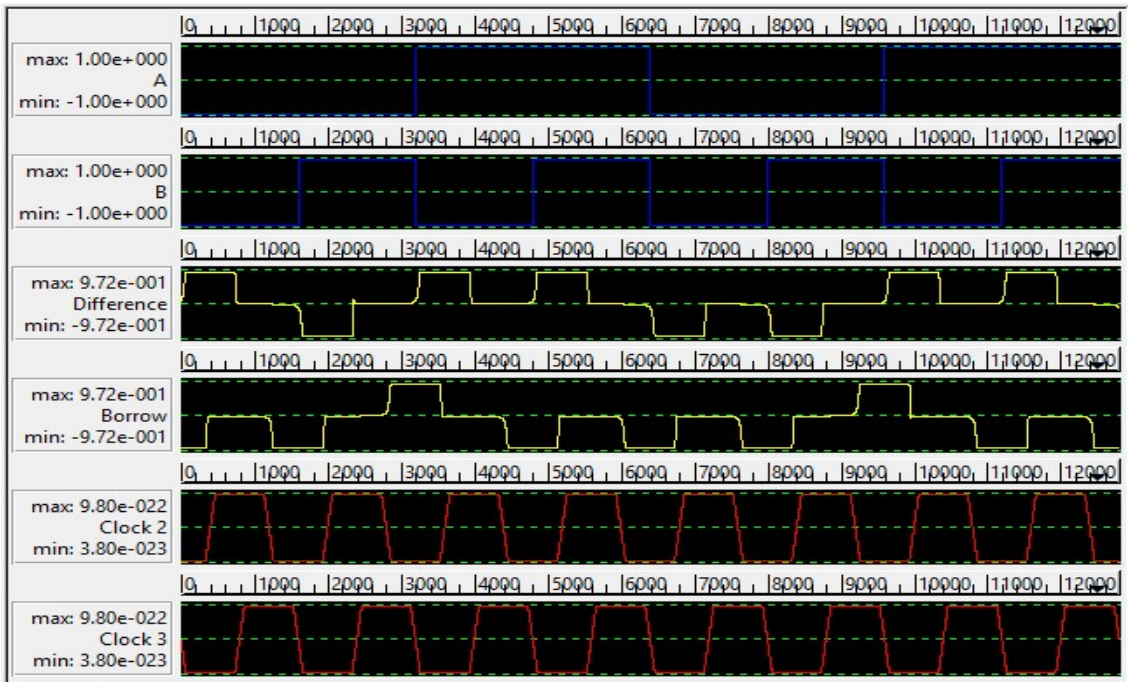


Fig. 9: Simulation results for proposed half-subtractor using 95 quantum cells

V. CONCLUSION

Quantum-dot cellular automata is a novel nanoelectronics-nanotechnology that promises very smaller size of digital circuits, very low power consumption, with high speed, minimum delay, high packaging density and operation at Thz (Tera-Hertz) frequencies are highly desired

features in the design and fabrication of digital logic circuits is considered as a resolution to the scaling problems in CMOS (complementary metal oxide semiconductor) technology. The multilayer QCA half-adder and subtractor are of importance to design arithmetic circuits. In this paper QCA half-adder and subtractor was introduced. The both half circuits are created the each quantum cell size 14×14 nm^2 with used the simulation in bistable engine. The cost is calculated by the equation 5, the half-adder cast is 0.045 and half substractor cast is 0.017. The presented half adder and substractor demonstrates significant improvements in terms of cell area, complexity, and robustness in comparison to old designs.

REFERENCES

[1]. Javeed Iqbal Reshi, M. Tariq Banday (2016) "Efficient Design of Nano Scale Adder and Subtractor Circuits using Quantum dot Cellular Automata" 3rd International Conference on Electrical, Electronics, Engineering Trends, Communication, Optimization and Sciences (EEECOS).

[2]. Razieh Farazkish, Samira Sayedsalehi and Keivan Navi (2012) "Novel Design for Quantum Dots Cellular Automata to Obtain Fault-TolerantMajority Gate" Hindawi Publishing Corporation Journal of Nanotechnology, pp. 1-7.

[3]. Biswas, P., Gupta, G., Patidar N., (2014). Basic Reversible Logic Gates and It's QCA Implementation, Int. J. of Engineering Research & Applications, 4(6), pp.12-16.

[4]. Sayedsalehi, S., Moaiyeri, M. H., Navi, K., (2013). Design of Efficient and Testable n-Input Logic Gates in Quantum-Dot Cellular Automata, American Scientific Publishers, Journal of Computational and Theoretical Nano science, 10, pp. 2347–2353.

[5]. Porod, W., (1997). Quantum-Dot Devices and Quantum-Dot Cellular Automata, International Journal of Bifurcation and Chaos, 7(10), pp. 2199.

[6]. Lent, C., S., Isaksen, B., Lieberman, M. (2003). Molecular Quantum-Dot Cellular Automata, J. Am. Chem. Soc, 125, pp.1056-1063.

[7]. Gupta, N., Patidar N., Katiyal S., Choudhary, K., K.,(2012). Design of Hybrid Adder-Subtractor (HAS) using Reversible Logic Gates in QCA, International Journal of Computer Applications, 53(15).

[8]. Patidar, N.; Gupta, N; Khabia, A.; K, Sumant & Choudhary, K.K. (2013). A novel 4-bit arithmetic logic unit implementation in quantum-dot, International Journal of Nanotechnology and Application (IJNA), 3(2), 1-8.

[9]. K. Navi et al. (2010). A new quantum-dot cellular automata full-adder, Elsevier Microelectronics Journal 41(12), 820–826.

[10]. Gupta, N.; Choudhary, K.K.; and Katiyal, S. (2013). Two Bit Arithmetic Logic Unit (ALU) in QCA, Int. J. on Recent Trends in Engineering and Technology, 8(2), 35-40.

[11]. C. Labrado and H. Thapliyal "Design of adder and subtractor circuits in majority logic-based field-coupled QCA nanocomputing" Electronics Letters 17th March 2016 Vol. 52 No. 6 pp. 464–466

[12]. Patidar. M., Gupta, N.: Efficient design and implementation of a robust coplanar crossover and multilayer hybrid full adder–subtractor using QCA technology. J Supercomput. 77(8), 7893–7915 (2021). https://doi.org/10.1007/s11227-020-03592-5

[13]. Khosroshahy, B.M., Moaiyeri, M.H., Abdoli, A.: Design and energy analysis of a new fault-tolerant SRAM cell in quantum-dot cellular automata. Opt Quant Electron 54, 593(2022). https://doi.org/10.1007/s11082-022-03992-2

[14]. Patidar. M., Gupta, N.: An efficient design of edge-triggered synchronous memory element using quantum dot cellular automata with optimized energy dissipation. J Comput Electron 19, 529–542 (2020). https://doi.org/10.1007/s10495-020-01457-x

[15]. Torres, F.S., Wille, R., Niemann, P., Drechsler, R.: An Energy-Aware Model for the Logic Synthesis of Quantum-Dot Cellular Automata. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. 37(12), 3031-3041 (2018).

[16]. Das, J. C., De, D. (2017). Nanocommunication network design using QCA reversible crossbar switch. Nano Communication Networks, 13, pp. 20–33.

[17]. Bahar, A. N., Roy, K., Asaduzzaman, M., (2017). Design and Implementation of 1-bit Comparator in Quantum-dot Cellular Automata (QCA). Cumhuriyet University Faculty of Science Science Journal (CSI). 38(1), pp. 146-152.

[18]. Sen, B., Goswami, M., Some, S., Sikdar, B. K. (2014). Design of Sequential Circuits in Multilayer QCA Structure. IEEE-ISED'13, International Symposium on Electronic System Design, pp. 21-25, doi:10.1109/ISED.2013.11.

[19]. Abdullah-Al-Shafi, M., Bahar, A. N., Ahmad, F., Ahmed, K. (2019). Performance evaluation of efficient combinational logic design using nanomaterial electronics. Cogent Engineering, Electrical and Electronic Engineering. 4(1), pp. 1-15.

[20]. Khosroshahy, B.M., Moaiyeri, M.H., Abdoli, A.: Design and energy analysis of a new fault-tolerant SRAM cell in quantum-dot cellular automata. Opt Quant Electron 54, 593(2022). https://doi.org/10.1007/s11082-022-03992-2

[21]. Norouzi. M., Heikalabad. S.R., Salimzadeh, F.: A reversible ALU using HNG and Ferdkin gates in QCA nanotechnology. Int. J. Circ. Theor. Appl. (2020). https://doi.org/10.1002/cta.2799