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LOW POWER EMBEDDED SYSTEM DESIGN

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ABSTRACT:
The growing popularity of embedded system has made designers to push more and more features into embedded systems. This has caused the issue of large power dissipation in embedded system. This paper proposes a technique for finding the sizes and the code allocation for the regions so as to minimize the total power consumption of the memory. To prevent overheating of devices researchers have been working on techniques for low power embedded systems. In this paper we prevent the study of memory design for low power embedded systems.
Keywords: *Cache power, leakage power reduction techniques, active switching reduction techniques, hybrid architecture memory, SPM and SRAM.*

1. INTRODUCTION

Power consumption is always a primary matter in embedded system today. As the size of the devices smaller and thinner, this constraint does not permit the system can integrate a large capacity battery for using in a long time. Power consumption and battery life is among the most critical concerns in light-weight embedded systems. In this paper we review some of the techniques introduced in designing low power embedded system. Power consumption is divided into two components, dynamic power consumption and static power consumption.

1. Dynamic power from logic signal switching activities.
2. Static power transistor leakage currents.

Dynamic power reduction can be classified into three categories with each category having a different focus: to reduce switching capacitance, to reduce switching frequency and to reduce supply voltage. We can save the total power consumption by concentrating the memory accesses on the low dynamic power region.

2. Structural Customization Approach

A system is a set of different functional components. At a design level there may be a set of components that form multiple choices. Such functions are called multiple choice functions.

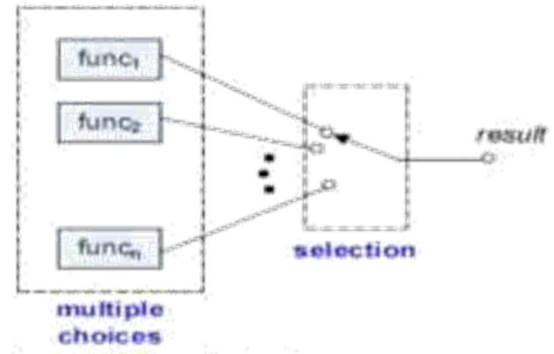

Figure 1. Multiple Choice Functions

At hardware level such structures can be modelled in as either tree structure or chain structures. In tree structure all the components are connected in parallel to the multiplexor. In chain structure the components are grouped and connected to smaller multiplexor. Numerous design techniques are necessary to reduce the active (switching) power and leakage power in memory design.

A. Leakage power reduction

Source biasing can be used where the array source node is isolated and biasing. This will reduce the leakage currents but will increase the access delay. The leakage power reduction will also increase the active power. In standby mode the leakage power is reduced. This will also reduce by switching off the power source. These techniques are also called as gated-VDD and gated-GND.

B. Active Switching Power reduction

Majority of switching power is dissipated in the data path where many parallel lines are activated. Smaller partitioning results in smaller bit line capacitance and lower active power as well as faster access time. For better efficiency the memory IO should be wide. The power consumption is high when the useful data present only in a small portion in wide IO. The power is wasted for sensing all the bits in the useful data. Cache hit rate will result in a significant power saving in embedded system. For sequential memory access pattern the data in wide IO will be at the output of the memory. This process will continuous when a new access is proposed into the memory. Whenever the cache hit rate increases the effective relative active power is decreases.

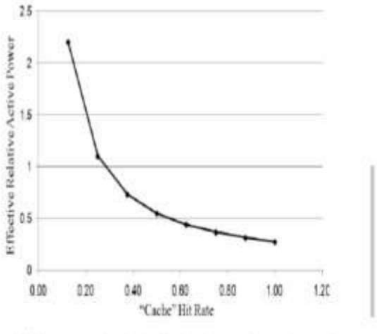

TABLE I
SPECIFICATION OF CACHE MEMORIES

Processor	M32R-II	
Clock Frequency	400MHz	
Temperature	348K	
L1 (Instruction)	The number of sets	128
	The number of ways	2
	Line size	16 byte
	Total size	32 KB
L1 (Data)	The number of sets	128
	The number of ways	2
	Line size	16byte
	Total size	32 KB
L2 (Unified)	The number of sets	256
	The number of ways	4
	Line size	16 byte
	Total size	128 KB

TABLE II
ACCESS DELAY AND POWER CONSUMPTION OF MEMORY MODULES

	Vdd [V]	P.O.	Delay [nsec]	leakage/cell [nW]	leakage/SA [nW]	SW_{bit} [J]	SW_{word} [J]
DP	0.75	HP	0.197	9.27	98.9	4.43e-14	3.38e-14
SP	1.2	MP	0.198	6.71	60.7	1.32e-13	1.40e-13

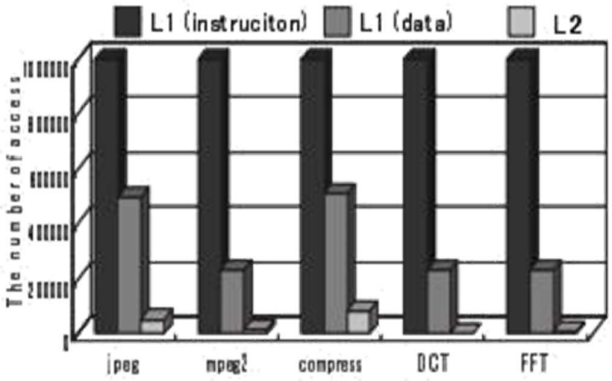

Fig. 2. The number of accesses to each cache

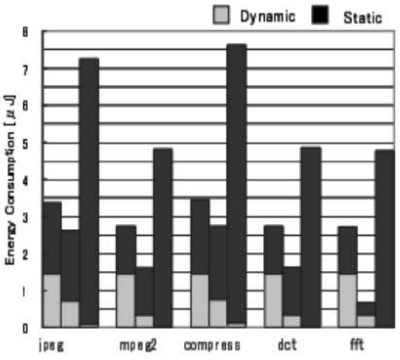

Fig. 3. Energy breakdown of DP-design

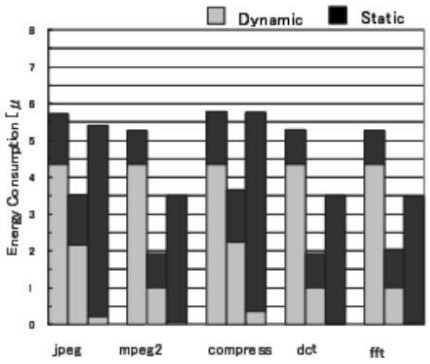

Fig. 4. Energy breakdown of SP-design

Related Work

In, non-uniform set-associative (NUSA) cache is proposed. The NUSA cache consists of one fast cache-way and several slow cache-ways. Unlike the NUSA cache, our hybrid memory does not suffer from such problems. The NUSA cache needs an extra mechanism for exchanging data to the fast and slow ways together frequently accessed data to the fast way. It causes a performance loss.

Our Approach

In this paper we apply the idea of our hybrid memory architecture to scratchpad memory(SPM).SPM is similar to cache memory.Both of cache memory and SPM consist of an SRAM. SPM consumes lower power than that of cache memory. SPM reduce the power consumption. SPM is widely used for not only to improve performance but also to reduce the power consumption. In this paper, we find functions and data objects which should be allocated

into the two regions of the hybrid memory. In this data objects include global variables and constants. In this paper we discussed about the leakage power reduction and active switching power reduction techniques to minimize the power consumption in the embedded systems.

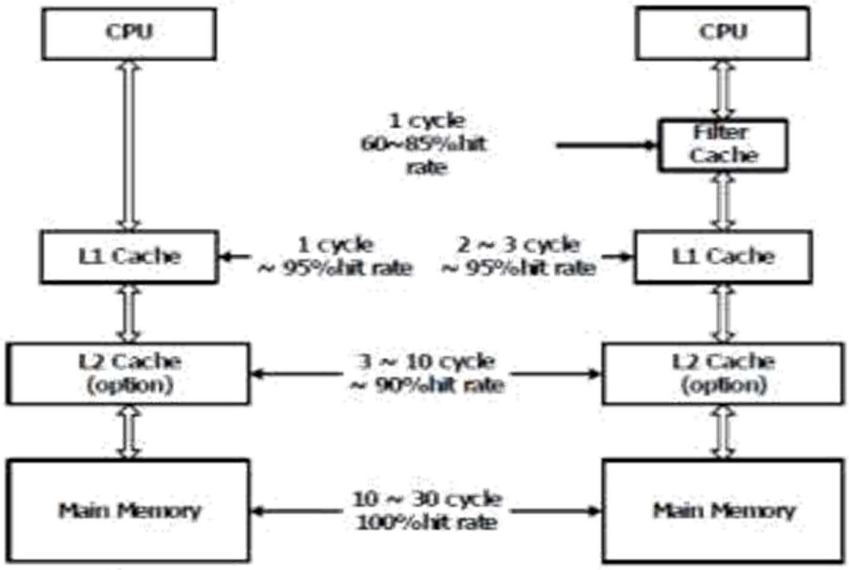

Figure 4 Filter Cache Structure

- **Cache parameters and locking in low power embedded systems:**

Cache run at speed almost as fast as CPU speed and improve system performance by reducing the effective memory access time. The memory order usually includes level -1 cache (CL1),level-2 cache(CL2) ,and main memory.CL1 is split into instruction(I1) and data(D1) caches and CL2 is unified. Improving predictability without decreasing performance of system. On the one hand, caches improve overall system performance. But on the other hand, caches increase overall energy consumption.

To decrease the energy consumption by cache:

- **Cache consumes a significant amount of energy in modern microprocessors.**
- **To reduce cache power, focus should be given upon reduction of both the power components.**

- Embedded microprocessor systems are nothing but computer chips that are integral part of lighting system.

- Embedded microprocessors are computer chips used inside devices other than computers to provide added functionality.

  Often in the areas of control and monitoring.

CONCLUSION:

Hybrid memory architecture is proposed for decreasing the on-chip memory energy consumption. The idea of the hybrid memory architecture is applied to SPM. Here we have mainly concentrated on cache memory related issues in design of low power consumption embedded system design. The results shows that hybrid memory architecture can save the total energy consumption by 49%.By preventing the leakage power and active switching power we can minimize the power consumption in the embedded system. We use cache for better system performance at the same time the cache consumes more power to reduce this more power we use a modern microprocessor in the embedded systems.

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