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ECG SIGNAL PROCESSING USING CODE RECOMBINATION ALGORITHM

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Abstract: An electrocardiogram (ECG) is used to record the electrical signal from the heart to check the functioning of heart conditions. The signals of ECG will be represented as waves on an attached monitor. Cardiovascular illnesses are identified using an electrocardiogram (ECG) signal processed using a Code Recombination Analog to Digital Converter (CR-ADC). The reduction in size of CMOS fabrication, delay rate, power consumption, noise and to increase the efficiency and accuracy of the ADC. This paper proposes the bidirectional pulsed-latches and non-overlap delayed pulsed clock signals which replace the existing master-slave flip-flops and 2-to-1 multiplexers to reduce the area and power consumption in ADC using code recombination algorithm. The CMOS fabrication of the ADC below 130 nm improves power efficiency. The prototype of CR-ADC implemented with a voltage source of 0.6 V, and a sampling rate of 10 kS/s, Signal-to-noise-distortion range (SNDR) and spurious-free dynamic range (SFDR) of the suggested ADC are 70.2 and 58.34 dB, respectively. It is more than 96% accurate compared to the Successive Approximation Register Analog to Digital Convertor (SAR-ADC).

Keywords: Electrocardiogram, Code Recombination Analog to Digital Converter (CR-ADC), Bidirectional shift register, Cardiovascular diseases.

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1 Introduction

Intelligent health tracking devices are required to satisfy the growing healthcare market's requirements and healthcare's own development. These devices identify abnormalities in biomedical signals using signal classification and artificial intelligence. a combination of hardware for handling AI and biomedical conversion is needed for conventional processors for biomedical processing using AI. The crucial component of the biological processed system of an ADC needs segmental data pre-processing capability and very low conversion power with less hardware overhead due to the limitations of storage and energy.

The algorithm of Code Recombination is used to process the ECG data. By using non-overlapping delayed pulsed clock signals and bidirectional pulsed latches in place of 2-to-1 multiplexers and master-slave flip- By utilising non-overlapping delayed pulsed clock impulse and bidirectional pulsed latches flops, space and power usage are reduced.

CMOS fabrication of the ADC should be lowered below 130 nm in order to increase power efficiency, improve precision, and reduce delay rates. Results indicate precision of more than 96%. A significant benefit in signal processing, storage, and computation is provided by the ADC feature.

The important part of electrocardiogram (ECG or EKG) signal waveform is QRS waveform denotes the ventricular depolarization of the heart. It consists of three deflections: the Q, R, and S waves.

The initial downward deflection observed in the complex is known as the Q wave. The initial upward deflection observed is referred to as the R wave. and is usually the tallest. Nearby the R wave, the S wave is a downward deflection. The Time period and morphology of the QRS waveform can provide important diagnostic information about the electrical activity of the heart and can help find various heart conditions. For example, a wide QRS complex can be a sign of a bundle branch block, while a narrow QRS complex is usually indicative of a normal conduction pathway.

The QRS typically lasts 0.08 to 0.10 seconds in people. An abnormal QRS pulse is one that lasts more than 0.12 seconds. The QRS complex must be accurately and fully captured in an ECG signal in order to be measured.

ECG devices should theoretically have a sampling rate of at least 50 Hz. A typical conversion rate for transducers inside ECG detectors is higher than 1 kHz, and actual ECG implementations have sampling rates of more than 500 Hz. Internal transducers in typical electrocardiogram (ECG) sensing devices must have a resolution of 12 bits at these sampling rates.

These speed and resolution requirements apply to general-purpose ECG monitors. High-resolution ECG detectors, however, are the only ones capable of finding some cardiac abnormalities. For instance, individuals with persistent ventricular tachycardia (VT) may experience tens of millisecond-long low-amplitude, high-frequency waves in the terminal QRS complex. According to the ECG result, these "delay potentials" are the product of the right ventricle's cells prematurely depolarizing.

. It takes sophisticated signal acquisition and processing methods using high- resolution sigma-delta () ADCs to make a signal that is essentially undetectable visible on an ECG.

Here, a power-efficient biological converter with the capability of data preprocessing called a code-recombination (CR) ADC is suggested. Architecture of data preprocessing in the analogue realm with little overhead to offer common feature extraction for biological AI processing, using a rough data compression method, transmission and storing costs can be decreased. a power-efficient biomedical processing design that is event-driven. When not stimulated, biological signals consistently display the characteristics of resting at their rest potential. The input is inactive in the sparse area, and the samples next to it have nearby or identical digital codes. There will be unwanted switching activity as a consequence of the ADC process.

By anticipating the MSBs with the highest capacitance, the Incremental Conversion Algorithm (ICA) lowers the switching power of DAC array and saves bitcycles per sample. If the assumption is wrong, the ADCs will reset the array and transform the input using the standard MSB first method, wasting power.

The Compressed Sensing Algorithm (CSA) offers the possibility of lowering the transmission rate. But because of the complicated implementation, signal recovery at the receiver requires more electricity.

A low power, monotonic capacitance switching-free 10-bit, 50-MS/s Successive Approximation Register analog-to-digital converter (SAR-ADC). Prediction changes the NSE into an NSPC scheme, which may not be able to increase the compression ratio based on the source. The major drawback is that they frequently overestimate or underestimate the number of components required.

The arrangement of the paper is structured in the following manner: Section 2 provides a discussion of the current methods, while Section 3 describes the suggested approach. The findings are examined in Section 4, and in Section 5, the final remarks are provided.

2 Literature review

Ki-Chan Woo et al. (2019) have developed a novel technique for building a bidirectional shift register that is space-efficient. This approach employs bidirectional pulsed latches in place of

master-slave flip-flops and 2-to-1 multiplexers, along with non- overlapping delayed pulsed clock signals, sub shift registers, and extra temporary storage latches. The proposed technique has been demonstrated to substantially decrease the size and power consmed by shift register. In their research, the authors created a bidirectional shift register of 256 bit using a 65 nm of CMOS fabrication, which had an area of 1943 μm2 and consumed 200 μW of power at a clock frequency of 100 MHz with VDD = 1.2 V. In comparison to traditional bidirectional shift registers, the new method reduced the space by 39.2% and power by 19.4%.

Mamun Bin et al. (2019) have developed a digital-to-analog converter (DAC) that is both speedy and accurate, and can be used in various readout applications within the wireless communication industry. The authors explain the configuration and tests of the DAC readout systems that are beneficial for radio frequency (RF) devices. The primary aim of this new DAC is to reduce power consumption. The system comprises a 10-bit DAC with a current routing design and an amplifier AB output in the high-swing category. The DAC was produced using a 130 nm process and consumes less than 0.6 mW of power. Hanie Ghaedrahmati et al. (2021) have presented a novel design for a continuous- time bandpass delta-sigma modulator (CT-BP-increment) that operates with low power consumption and high speed, making it suitable for use in nanoscale CMOS technology. The design uses a self-biased inverter-based amplifier instead of conventional op-amps in an integrator configuration. The modulator also employs a 5-bit asynchronous successive approximation register (ASAR) quantizer. The proposed modulator achieves a dynamic range (DR) of 61 dB and a signal-to-noise-and-distortion ratio (SNDR) of 58 dB when operated at a 400 MS/s sampling rate, 30 MHz bandwidth, and 100 MHz intermediate frequency (IF), while consuming only 2.5 mW from a 1V supply. The core area in 28 nm LP CMOS is 0.04 mm², and it achieves a figure of merit of 38.6 fj/Conv.-step.

Lingxiao Shen et al. (2020) developed a 10 billion (10b) analog-to-digital converter (ADC) that operates at 50 mega samples per second using TSMC 0.18 μm technology. They utilized a redundant capacitor digital-to-analog converter (DAC) to enhance the accuracy of the comparator. The ADC employs two-edge synchronous asynchronous clocks with alternate comparators to minimize kickback noise and achieve high speed. The team also proposed foreground and background calibration techniques based on the comparator offset to improve the performance of the structure.

Xuan Zhou et al. (2019) proposed that as the demand for aerial remote sensing grows in both domestic and millitay domains, Synthetic Aperture Radar (SAR) systems with high resolution, wide range, and multiple modes need to be developed. The Omega- K algorithm is found to be more merites in terms of quality and accuracy among the available imaging algorithms. However, the STOLT interpolation, which is a vital component of the Omega-K algorithm, is complex and poses a challenge for traditional hardware description languages (HDL) due to their weak ability to express algorithms, long programming cycles, and low simulation verification efficiency. To address this issue, the authors suggest an approach based on high-level synthesis (HLS) to realize the Omega-K algorithm. This involves designing a parallel processing architecture and optimizing array storage and flow processing using HLS. The proposed approach is expected to efficiently achieve high-accuracy SAR imaging on the processing platform of field programmable gate array (FPGA).

3 Proposed System

The principle purpose of this investigation is to add characteristics and acquire superior qualities of biomedical images for the correct analysis. It is suggested to use the CR-ADC, a biopotential converter with an energy-efficient data preparation feature. It has these characteristics:

To provide a common feature extraction for biomedical AI processing, The analogue domain is used in the creation of data preprocessing, with little overhead. a method of approximating data compression that lowers storage requirements and transfer costs. a power-efficient biomedical processing design. Pulsed latches are used in the bidirectional shift register in place of master-slave flip-flops to minimise space and power consumption. The Architectural block diagram of CR-ADC is shown in Fig 1.

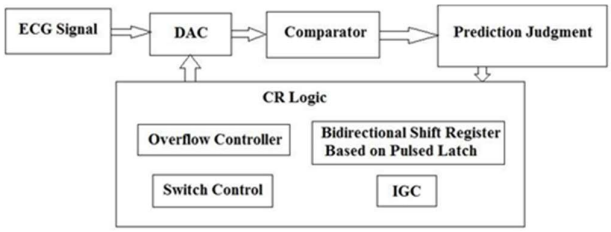


Figure 1 Proposed Architecture

The Wireless Sensor Network (WSN) offers a significant benefit for the upcoming generation of health monitoring applications. Unlike traditional ADCs that use Nyquist sampling, LC-ADC employs a sparsity of signals to capture low-power data.

3.1 Code Recombination-ADC

The input sound is sampled into digital code using N bitcycles in the N-b SAR- ADC. The transducing procedure activates all of the ADC's components. The signal's sparse characteristics allowed for the further reduction of power usage. The test potential is produced when the DAC array swapping is controlled by the IGC and prediction range
VR is delineated as

$$V_R = \frac{2 \times V_{Ref}}{2^M} \quad (1)$$

Where, V_{Ref} - reference voltage of DAC

M - number of predicting MSB

Where, $VRef$ - reference voltage of DAC M - number of predicting MSB

If the predicted MSBs match the earlier samples, multiple redundant switching verifies this. There might be variations from bit to bit in the digital result. Therefore, it is not power-efficient to continuously look for the same MSBs.

3.1.1 Operating Principle of CR-ADC

A-10 bit DAC, one prediction judgement block, a dynamic comparator, and one CR logic block make up the suggested CR-ADC. When a signal is digitised using variables such as the binary code factor, original guess code D, and updated guess code D, CR logic has the benefit of

producing multiple comparison results. For the purpose of shifting binary data on both sides, a bidirectional shift register is used. A 4-bit stream of data K for data compression and pathological detection is also provided by CR-ADC in addition to the output of 10-bit digital code at high efficiency.

There are three phases that make up the CR-ADC quantization process. These segments are P1, P2, and P3. The CR-ADC quantization operating concept is described using a 5-bit ADC. The DAC array's initial test potential and forecast interval are generated by P1 final sample digital code. The comparator contrasts the finished sample with the current input. Direct capacitor CR1 switching is the comparison's result. The initial two comparison output is opposite, Once the incoming signal is verified to be within the prediction interval, conversion is complete. As a result, for the given input, the final sample and its associated digital code are identical. If not, based on the outcome of the subsequent comparison, The present sample's placement within the tracking frame is determined. And the capacitor CR1 is swapped (SR1). The tracking window, which is used to manage samples with possible differences under 1 LSB but that are related to nearby digital code, on either side of the prediction interval is distinct. SR2's voltage swing is twice as large as SR1's, so be mindful of that. As a consequence, the test potential of SR2 is situated at the border of the tracking. If the 3rd comparison's results differ from those of the first two, and the digital code of the sample is changed by rectifying code "01," The tracking frame's sample is a reliable one.Along with the subsequent initial guess code, the current output code is also renewed.

Table 1 Lookup Table for the Correction Code

Conditions	$D_1 \oplus D_2$	$D_3 \oplus D_4$	D_{final}	D_1	*Correction Code*
1	1	*	*	*	+0
2	*	1	0	*	+01
3	*	1	1	*	-01
4	0	0	0	0	-10
5	0	0	1	0	-01
6	0	0	0	1	+01
7	0	0	1	1	+10

The input is presented as P2, because it is outside the tracking window provides specifics on the SBP and SFP's operating principles. The input's smallest valid subrange is first determined by starting the binary search forward process (SFP). Using a BCF that is progressively shifted with the starting value set to "00... 010," the test potential sequence is produced throughout SFP and SBP.

The original guess code BCF and D are added to produce the first test voltage in SFP.

$$D' = D + \text{“00…010”} \quad (2)$$

A bidirectional shift register is used to acquire the Binary Code Factor (BCF), and there is only one "1" in the series of the BCF. K Data begins forward-searching while numbering. If the comparison result remains the same, the "1" in the BCF is incrementally shifted to the left by single bit after each comparison cycle, and the following test potential is calculated by adding the updated BCF and the most recent estimate code D in order to increase the search window.

The Search Backward Procedure (SBP) is triggered when the output is reversed, and data K are captured In particular, until the BCF returns to "000... 01," The sum or difference of the progressively right-shifted BCF and the updated guess code D determines the test potential series in SBP, depending on the comparison outcome.

The P3 digitalizes the outgoing digital data. The seven criteria and the five adjustment codes are used, as shown in Table I, to fix the conversion error caused by redundant switching. While D1, D2, and D3 are the results of the first three comparisons, correspondingly, D final is the result of the final comparison.

The comparator noise, reference noise, and comparator kickback noise all have a significant impact on forecast accuracy. Even though comparator noise must be reduced to less than 1 LSB, it set the minimal prediction range. whereas reference noise may alter the prediction range arbitrarily leading to inconsistent prediction. If the resolution is lower, the comparator noise will be bigger. Additionally, during comparison, the top plate potential of the DAC array would shift due to kickback noise from the preamplifier's output node. The kickback noise may cause Because the input voltage is low in the initial comparisons cycles that the ADC will quantizes the incoming signal with minimal activity, the comparison results will be inverted. The input pair for the preamplifier is thus meticulously designed to reduce kickback noise and comparator noise. Additionally, the comparatively large 65 fF unit capacitor is used to further muffle kickback noise.

3.1.2 Overflow Operation

The corresponding full adder may overflow since D and BCF are added to produce the test voltage series throughout SFP. With an initial guess code of "10110," input Vi with interval coded "11110." as shown in Fig. 6. D "11100" should be added to BCF "01000" during the sixth comparison interval to create the following test potential. The overflowing adder is filled. Decrease the search area even in SFP, the "1" of BCF is meant to shift to the right successively, in order to accurately locate the subrange of those inputs. Additionally, the updated D is reset to the previous number once overflow is discovered, and K data are noted. The BCF creates the right-shifted number in the meantime, which in this case is "00100." The DAC array and comparator are not turned on until the detection of overflow in digital blocks has been finished. The SBP is used to finish the conversion by iteratively repeating the previous procedure till D is not overflowing.

3.1.3 K Data Analysis

To characterise the activity of the input, the CR-ADC generates a data flow of K values. K data are susceptible to the leftover of the subsequent sample during quantization. K only requires a few bits to capture and is constrained by the ADC's resolution. serving the same purpose as the amount of SFP.

$$2K \geq N \tag{3}$$

where N is the resolution of the ADC. To facilitate the process to transfer, process, and store the data, it is compressed and extracted. Data K, however, does not precisely match the voltage leftover among observations.

$$2^{K-1} \leq | X(N+1) - X(N) | \leq 2^{K} \quad (4)$$

where X(N + 1) and X(N) refer to consecutive samples, i.e.,

$$| X(N+1) - X(N) | = 2^{K-1} - x2^{K-1} \quad (5)$$

where (x2K-1) is the fuzzy factor.

If the input X(N) fulfils the aforementioned equation, K would be the equivalent feature. In order to retain enough vital info for further handling while lowering reduction costs, the fuzzy factor is disregarded. The fuzzy component increases as K increases. The QRS complex, which is the primary component of ECG transducing and does have the greatest range, which increases the K number. A fuzzy factor would therefore exclude the disturbance found in QRS peaks in order to generalise the feature.

3.2 Bidirectional Shift Register

Bidirectional shift-registers have a wide range of implementation, such as digital DC/DC buck converters, decompressors, low dropout regulators (LDO), and delay-locked loops (DLL). These shift registers typically consist of N number of master-slave flip-flops and 2-to-1 multiplexers, and are N bits in length. When the direction indication is "1," the data (Q) is shifted to the right, while it is shifted to the left when the direction indication is "0".

The master-slave flip-flops and two locks that are used in the traditional bidirectional shift register. To reduce the size and batter drainage of the device, it is suggested to use a pulsed clock signal in place of master-slave flip-flops and pulsed latches consisting of a latch. However, using all pulsed latches at the same time during the clock pulse width causes a race situation, so a bidirectional shift register with pulsed latches cannot utilize a pulsed clock signal. As a result, a bidirectional shift-register with pulsating latches is unable to right- or left-shift the data. This issue was resolved by the shift register using pulsed latches by adding extra temporary storage latches and sub-shift registers. Even if 2-to-1 multiplexers such as the typical bidirectional shift register are added, the reverse order pulsed clock impulses prevent it from shifting the data left. In order to maintain the input signal, a lengthy hold period is also necessary.

Here, a bidirectional shift register with a small footprint using bidirectional pulsating latches is suggested. Bidirectional pulsed latches that have been suggested can be used to move the data right or left.

By proposing bidirectional pulsed latches and non-overlap delayed pulsed clock
signals in place of master-slave flip-flops and 2-to-1 multiplexers, it lowers the area and power consumption. Additionally, the hold period is decreased to a clock pulse width.

4 Results and Discussion

The 0.13-m CMOS technology was used to make a 10-b CR ADC. The CR-ADC core is 0.11 mm2 in size. The intended sampling frequency is 10 kHz. To make the analogue blocks easier

to understand and maximise the inputs accessible, the VR = Vdd. Additionally, the two redundant capacitors limit the ADC's input range to 97% of its maximal swing.
The simulation of the output signal generated in the moniter which is shown in Fig 2. It consist of output ECG signal and k-output and digital output for the corresponding input signal database.

Figure 2 Simulated Waveform

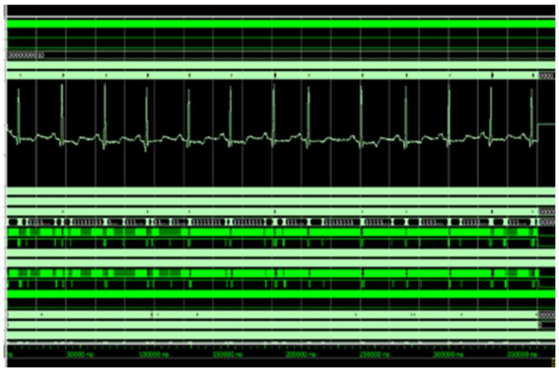
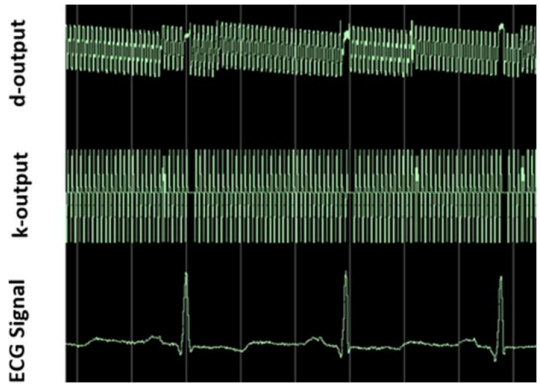


Figure 3 Comparison between output digital ECG signal and K-output signal



The evaluated outcomes of a 1/2 full-swing ECG signal with consumed bitcycles and K records from the MIT arrhythmia database. The input characteristic is shown using K data in a data-rate-reduction manner. Additionally, compared to a standard 10-b SAR ADC, the average bitcycle usage and bit occupancy of K are 2.46 and 2.5 times lower, respectively.

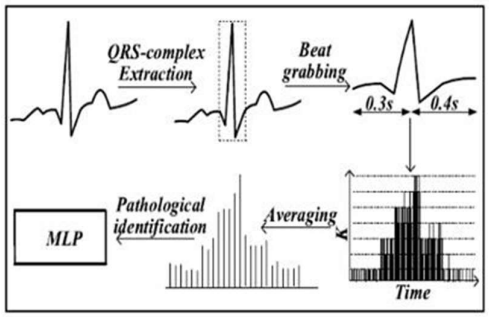
The quantization uses more than ten bitcycles, the input frequency is greater than 100 Hertz, and the ADC's power increases significantly. With a rise in input frequency, The voltage ratio of the digital circuit and comparator increases. The Walden figure of merits describes it as (FoM),

$$FoM = \frac{P}{f_s \times 2^{ENOB}}$$

where P represents the ADC's power usage for an incoming sine waveform. The study involved the computation of the FoM value using three different sinusoidal input rates: 1 kHz, 100 kHz, and 4.91 kHz. The results showed that all the examples fell within the expected range of

prediction when the input was near to dc. Despite the input frequency being greater than 1 kHz, the encoding method usually required more than 15 bitcycles.

Figure 4 Stages in ECG processing



A system for identifying specific cardiovascular diseases is suggested as a test of K's feature extraction capability. The MIT arrhythmia database's QRS complex is first recognised and converted into pulses. Every 0.7s beat was translated to the equivalent K- data in Fig 4 Nearby ten segments of K are averaged to further reduce data usage and generalise features. For pathological identification, the structural characteristic is then passed to a multi-layer perceptron (MLP).

Table 2 Comparison and Summary

Specification	*SAR ADC [15]*	*CR ADC*
Technology	180nm	130nm
Resolution (bits)	12	10
Supply Voltage (V)	1.5	0.6
Unit Capacitor (fF)	2.6	65
Sampling Rate (S/s)	40K	10K
Power (μW)	0.8-2.3	0.04-3.8
FoM (fJ/Conv.-step)	9.1/28	6/13.4/56.6
Core Area (mm^2)	0.167	0.11
Total Power Supply (mW)	144	127

Table 2. describes the comparison between the SAR-ADC and CR-ADC.

5 Conclusion

For the acquisition of biomedical signals, a 10 b CR-ADC in a 0.133-m CMOS fabtication was suggested. With the least amount of hardware overhead, Searching Backward Procedure (SBP) and Searching Forward Procedure (SFP) are used to optimise power efficiency during both burst like periods and low activity periods. Analyses are done on the DAC's loading and switching ability. Due to its event-driven design, CR-ADC has the ability to identify the signal's characteristic. Additionally, a brand-new K-data feature description technique is suggested and demonstrated for use in pathological identification. It is more than 96% accurate.

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